

# B450 GAMING X

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[illegible]

**Model Name:B450 GAMING X**

### Component value change history

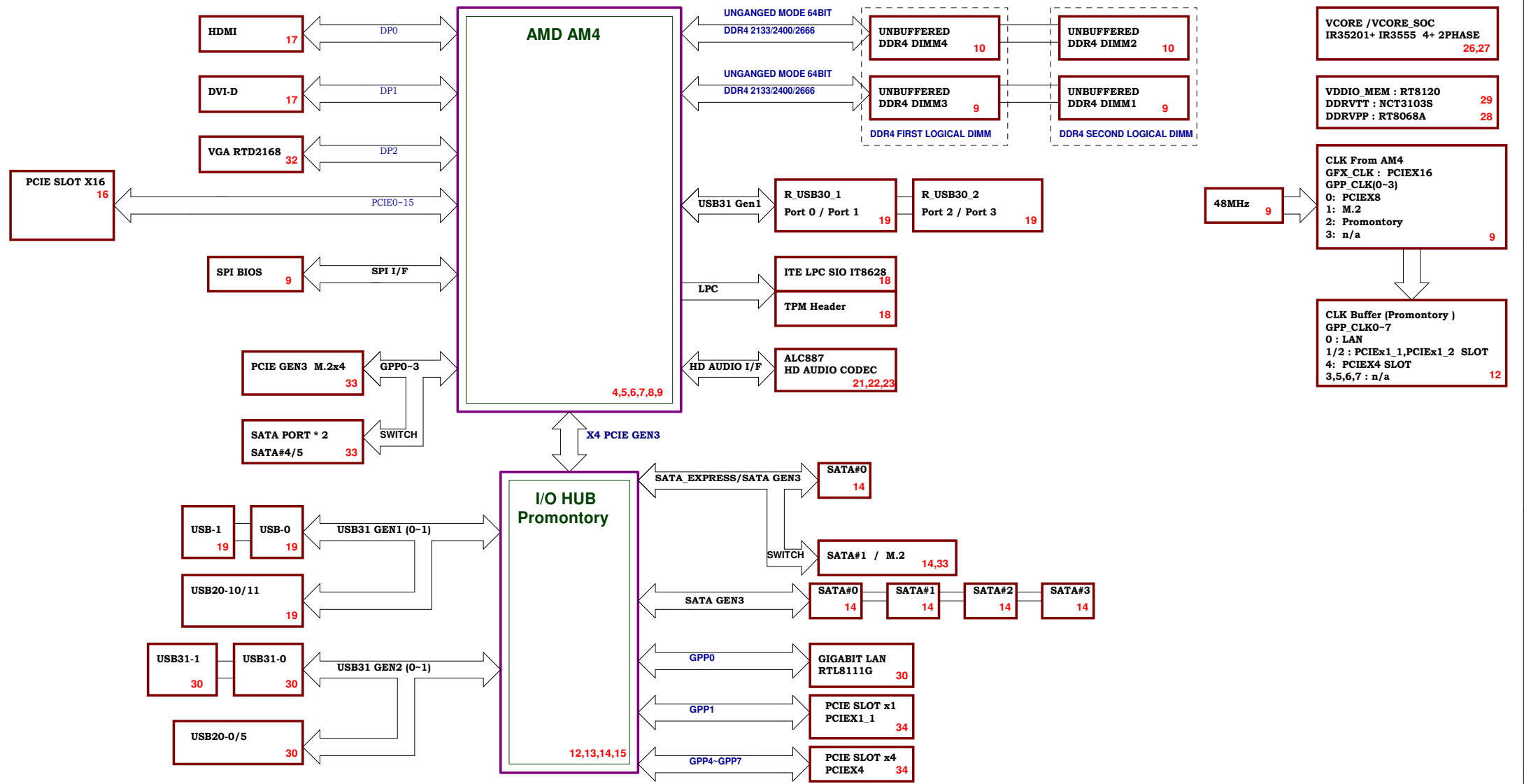
**Version: 1.1**

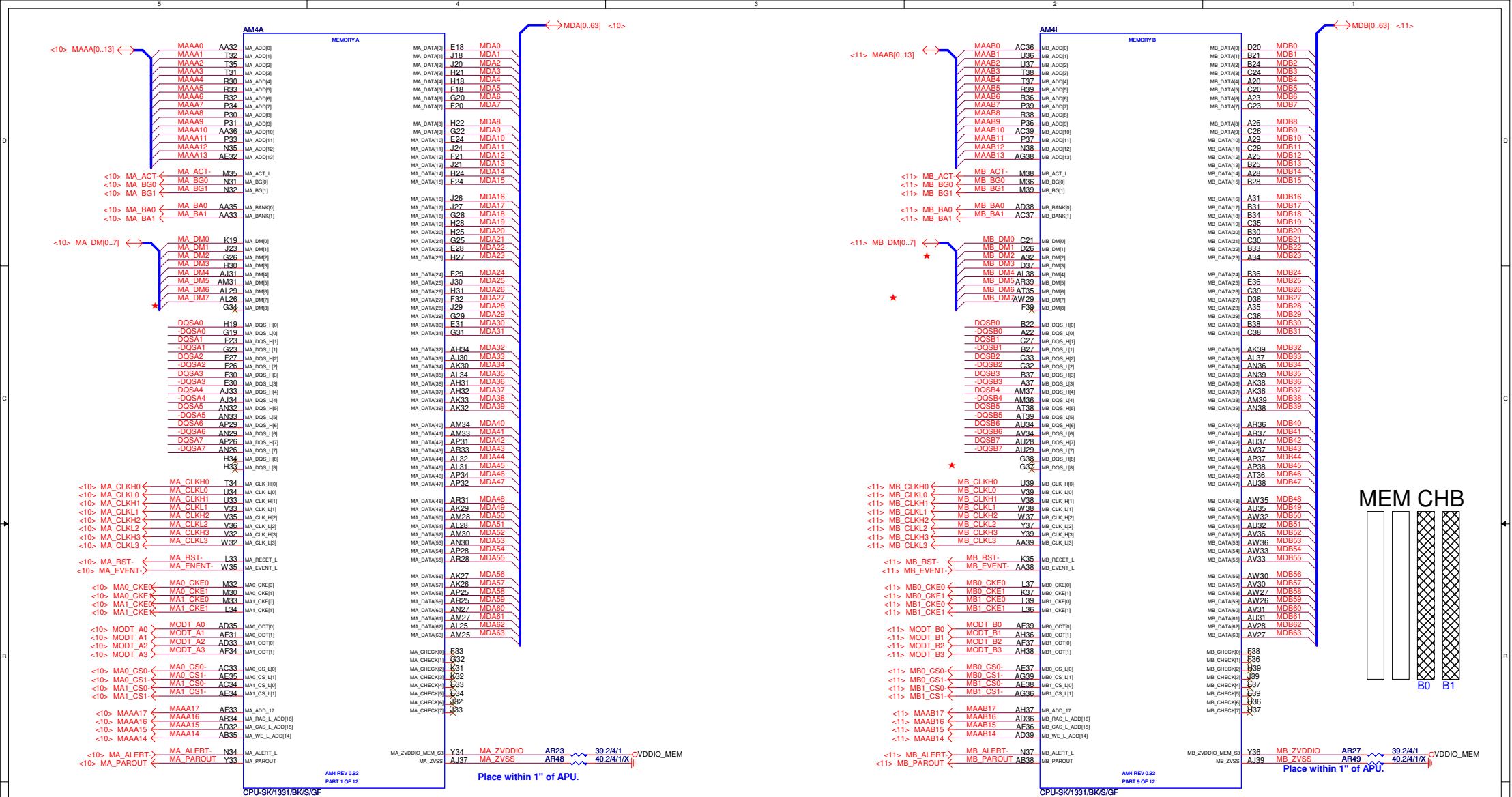
**P-Code: U98126-0**

[illegible]

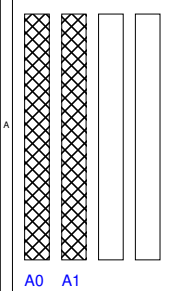
**Circuit or PCB layout change for next version**

[illegible]

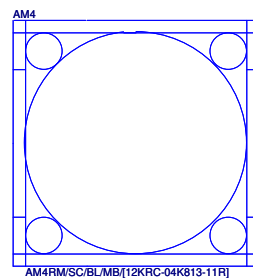




MEM CHA



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**GIGABYTE™**

**APU DDR4**

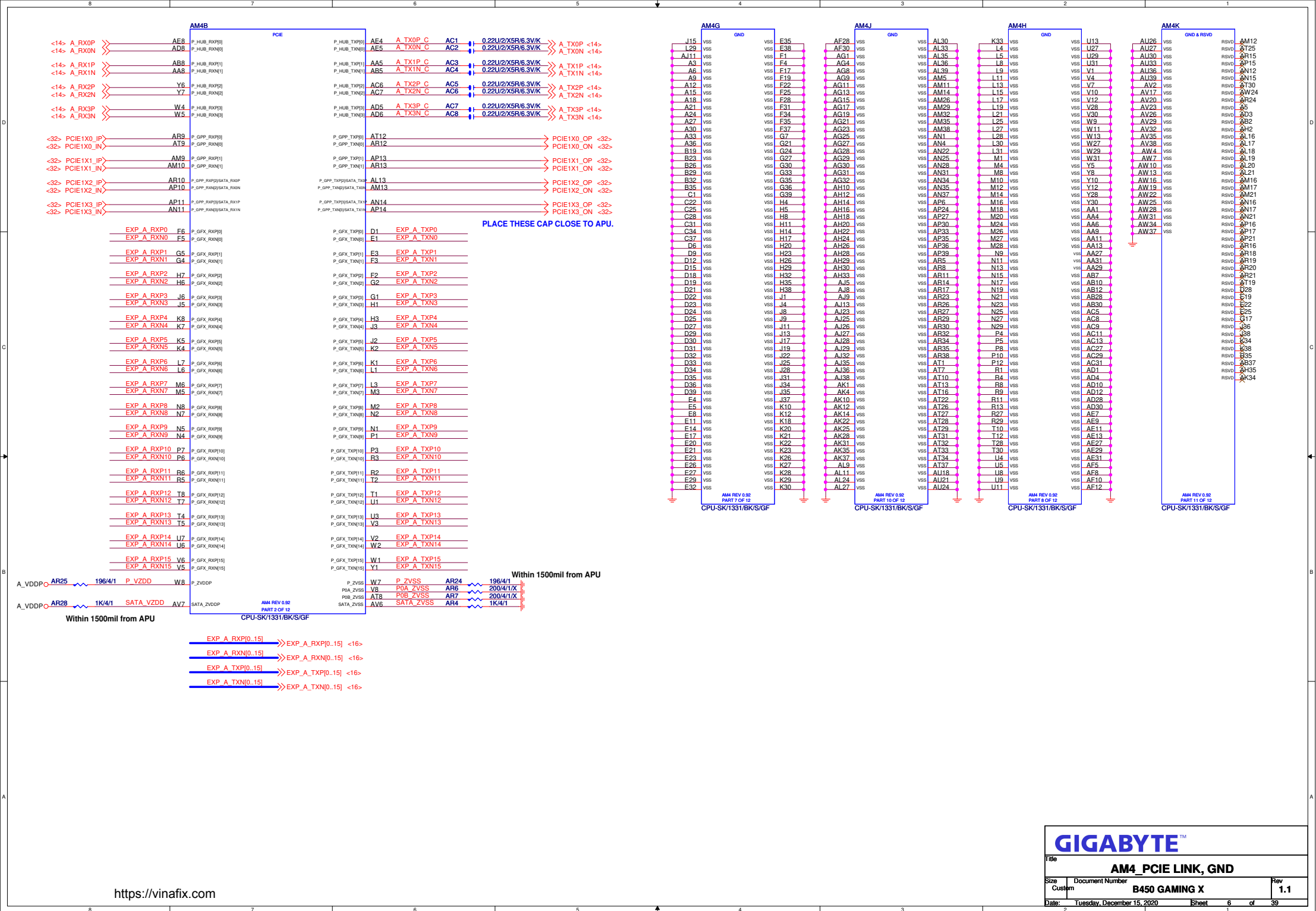
**B450 GAMING X**

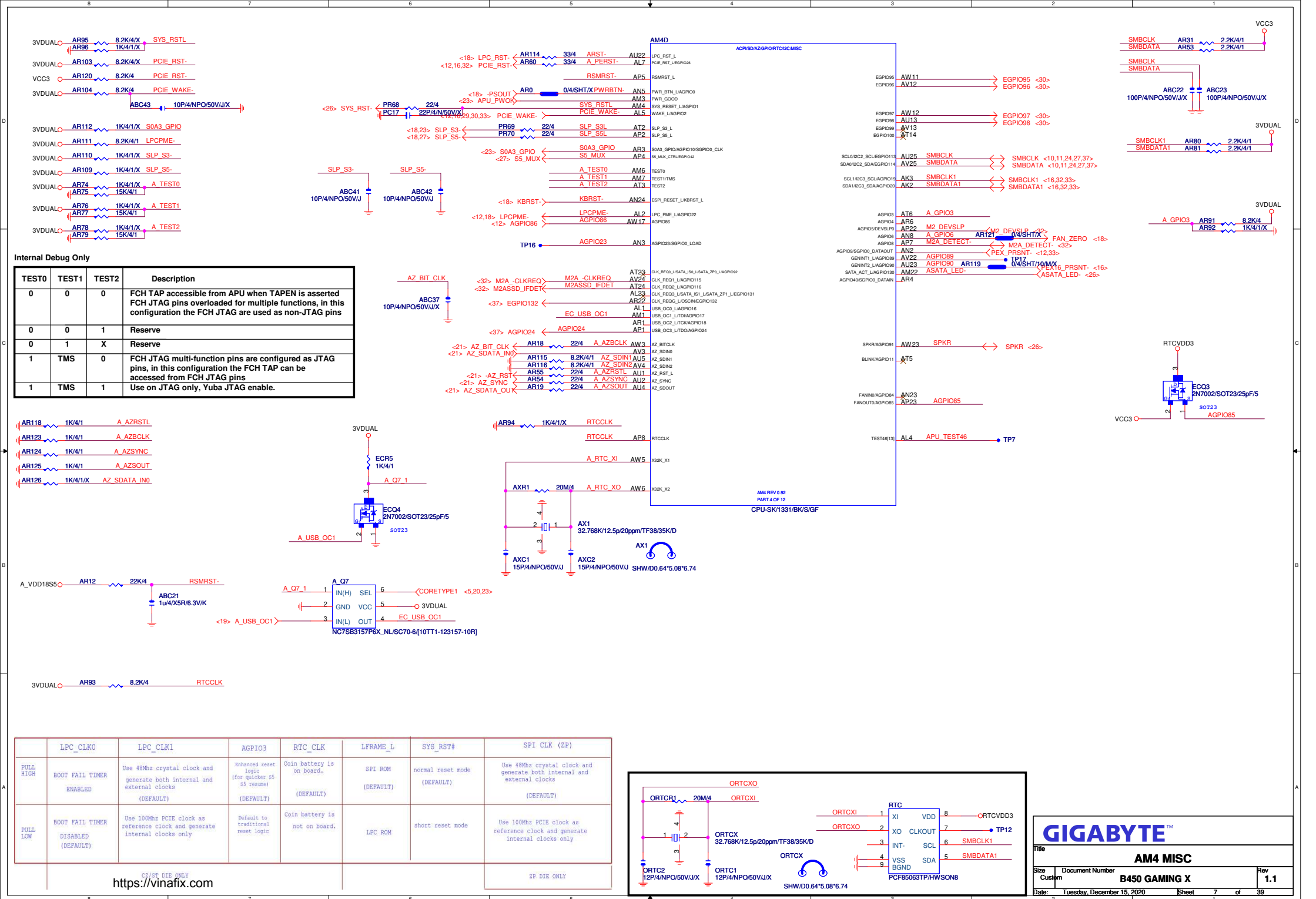
**Rev 1.1**

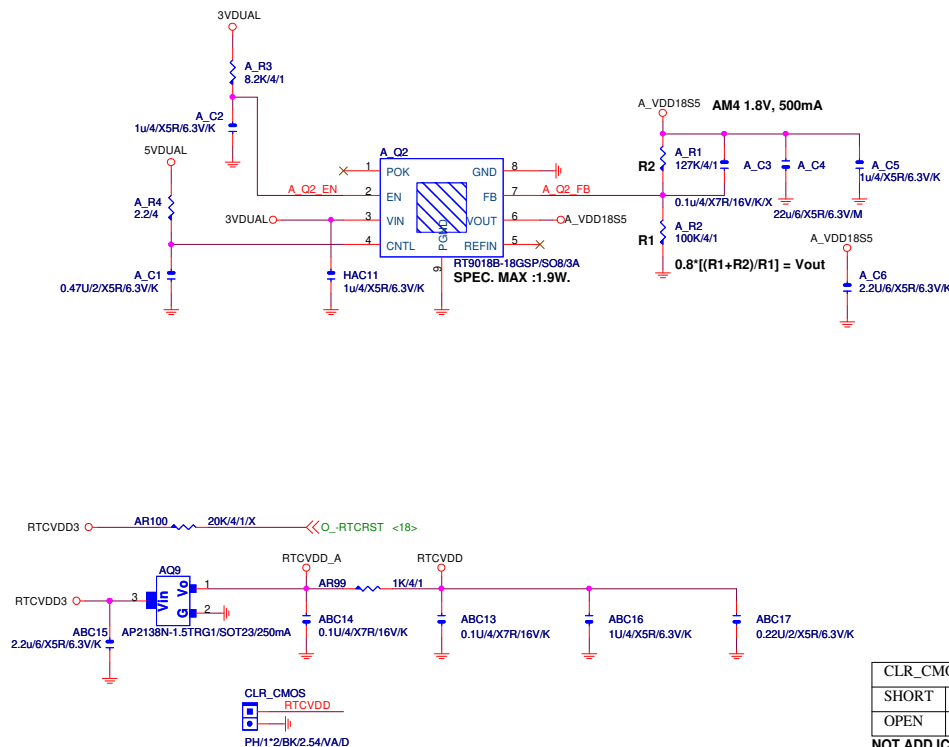
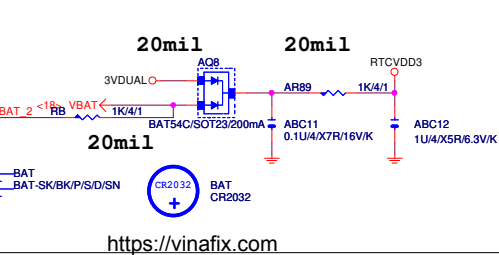
Date: Tuesday, December 15, 2020 Sheet 4 of 39

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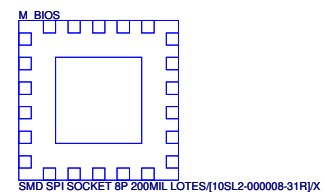
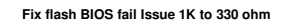


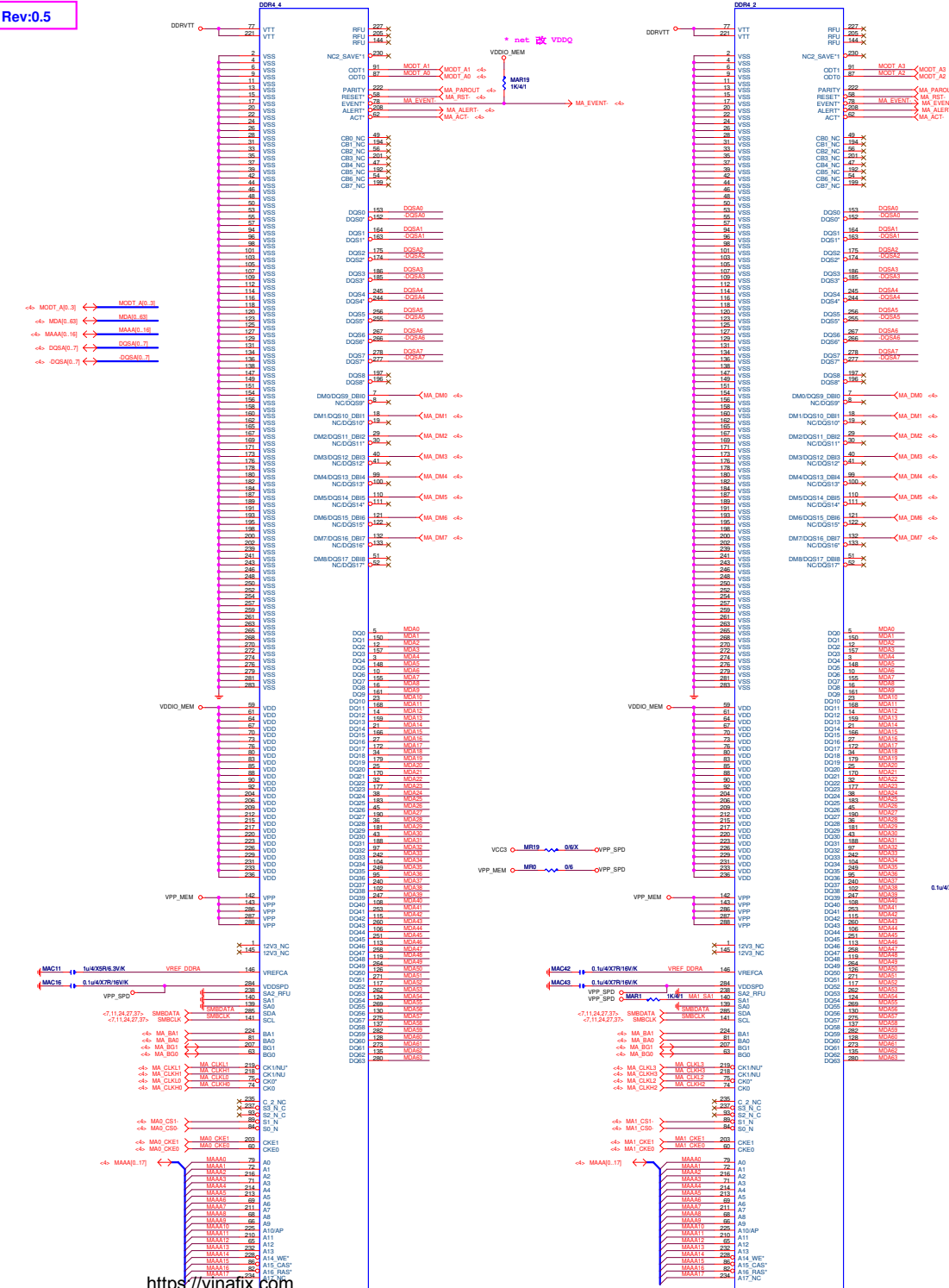


CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

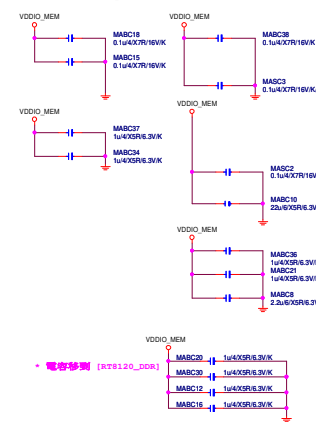
**NOT ADD ICT FOR RTCVDD PIN**



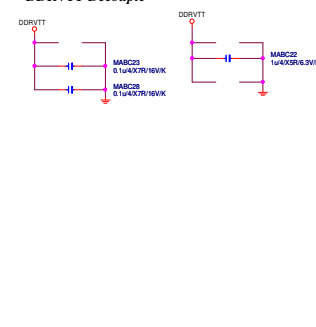




DDR12V Decouple



DDRVRTT Decouple



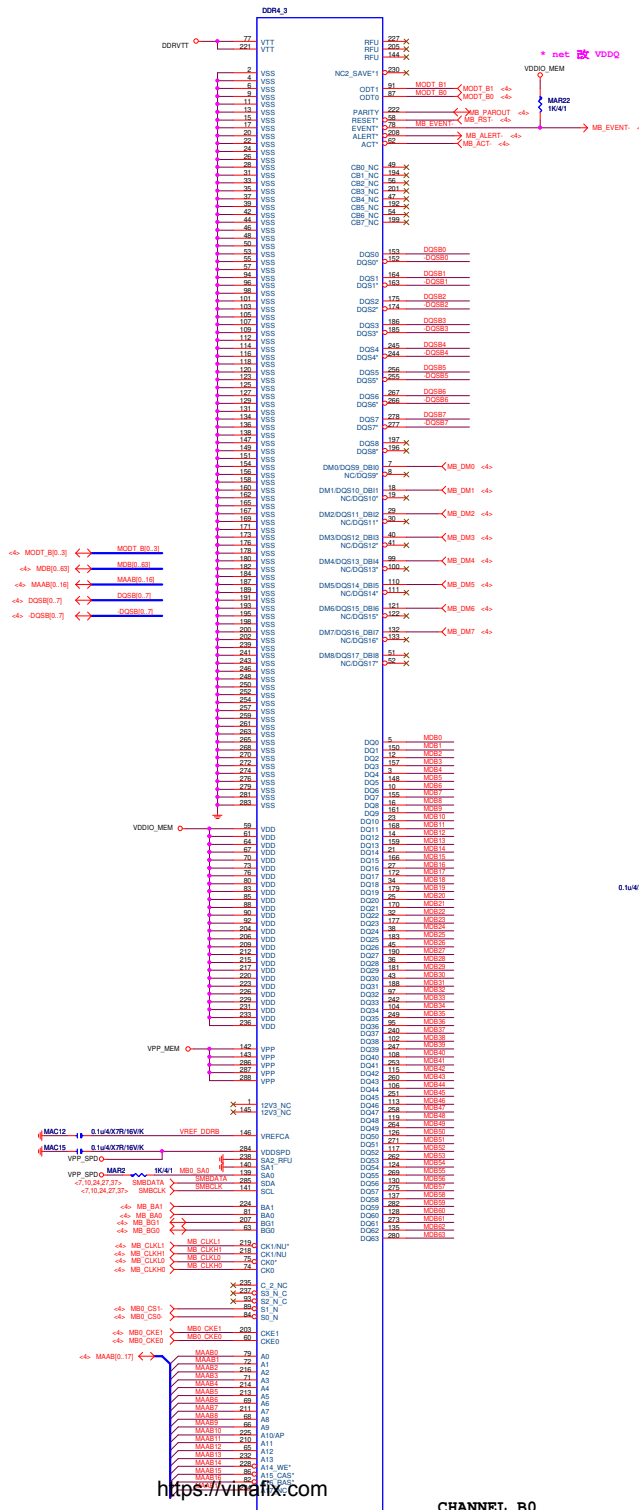
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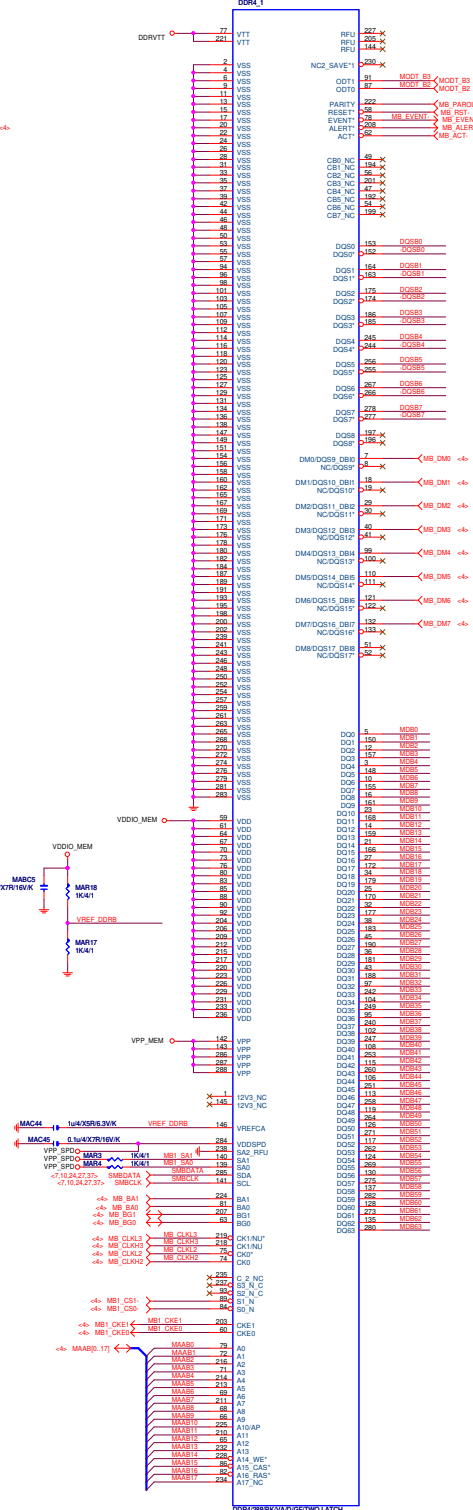
CHANNEL A0  
SA2:0=000

CHANNEL A1  
SA2:2=010

GIGABYTE		
DDR4 CHANNEL A		
Size	Document Number	Rev
1.1	B450 GAMING X	1.1
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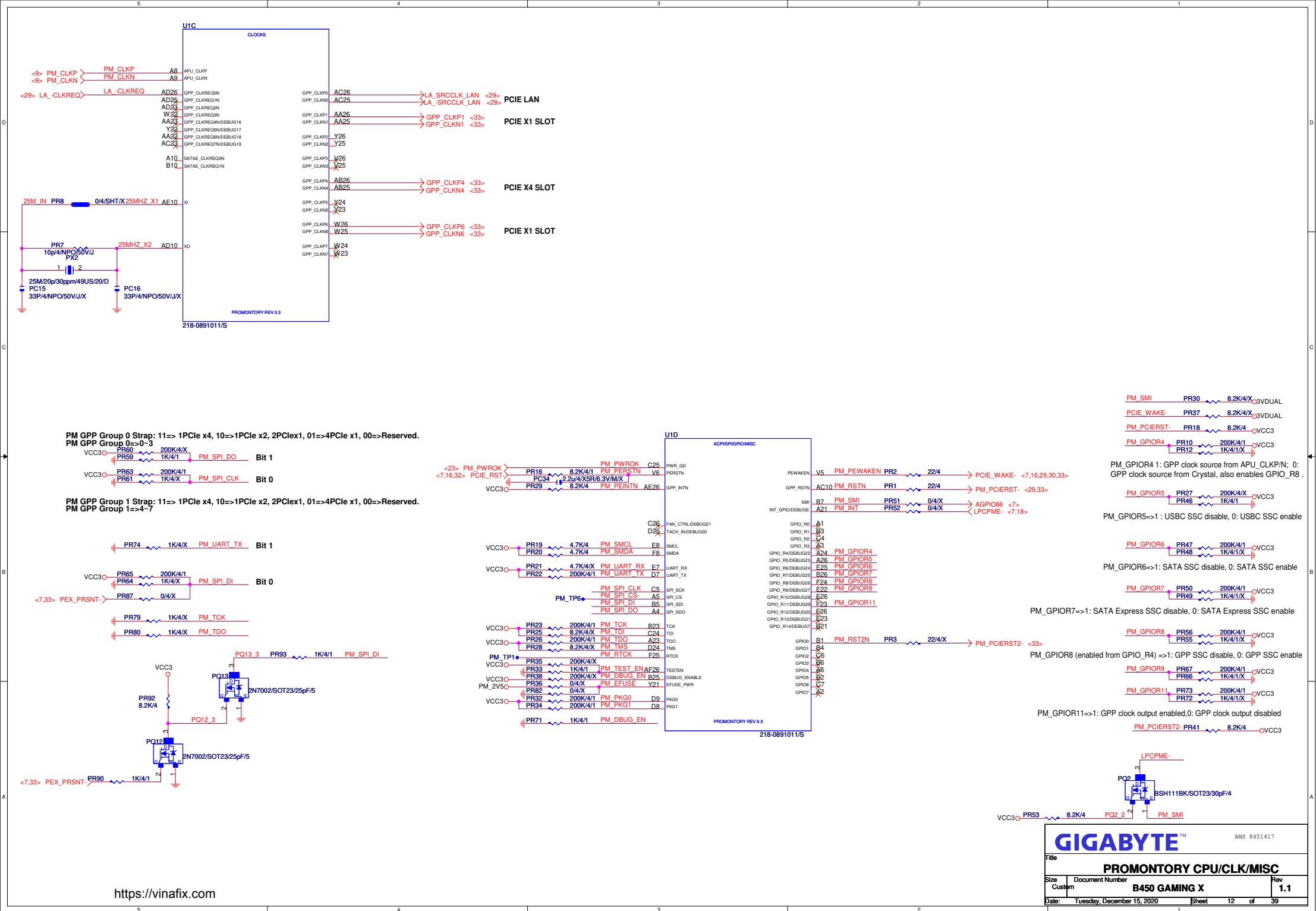


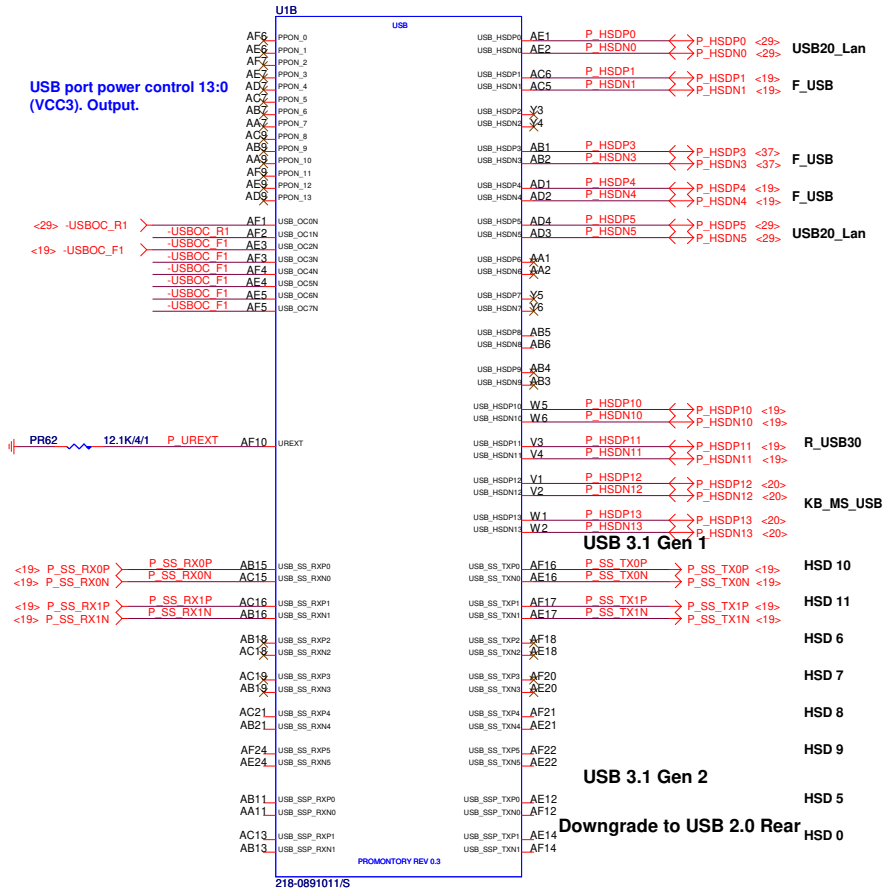
CHANNEL B0  
SA2:1=001



CHANNEL B1  
SA2:3=011

<b>GIGABYTE</b>		
DDR4 CHANNEL B		
File	Document Number	Rev
	B450 GAMING X	1.1
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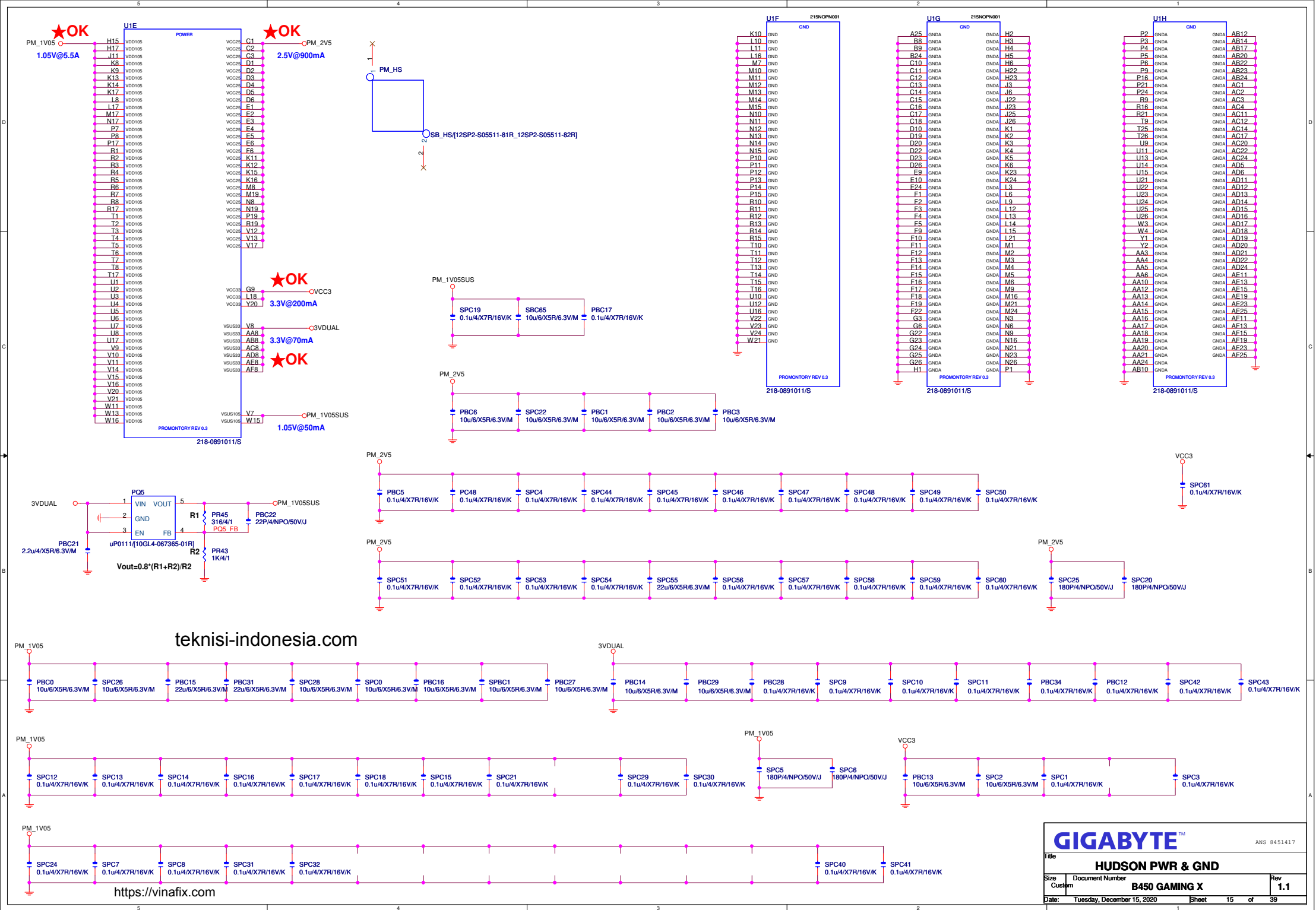
USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	USB2.0	USB_OC
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

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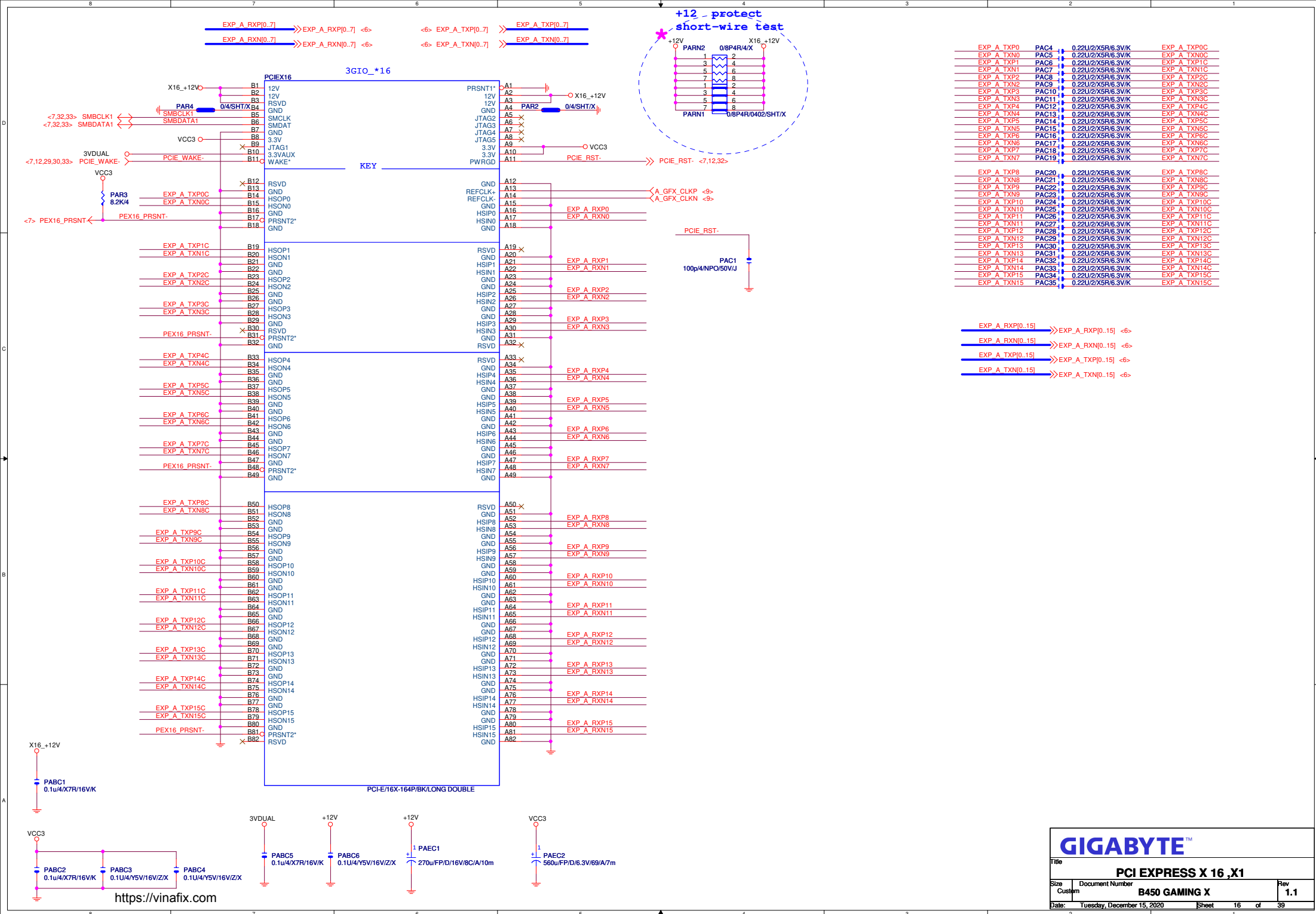
BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

GIGABYTE™				ANS 8451417
Title PM USB				
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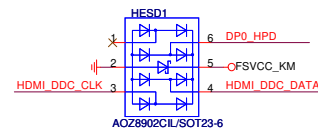
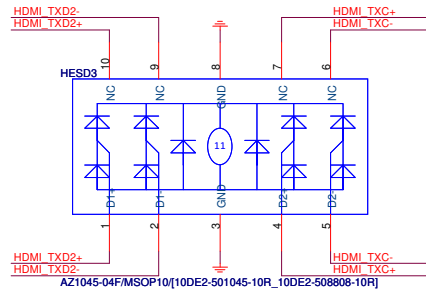
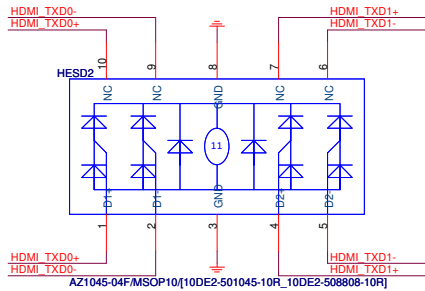
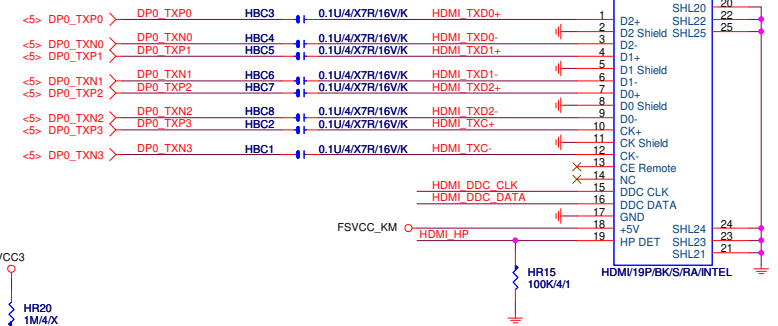
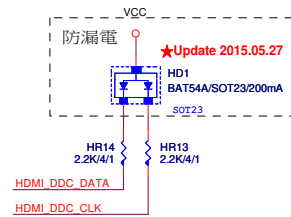
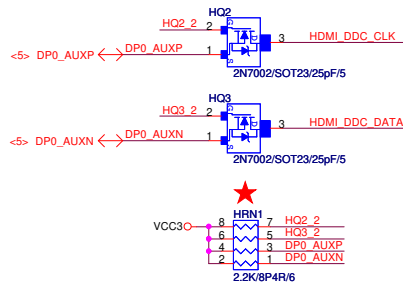
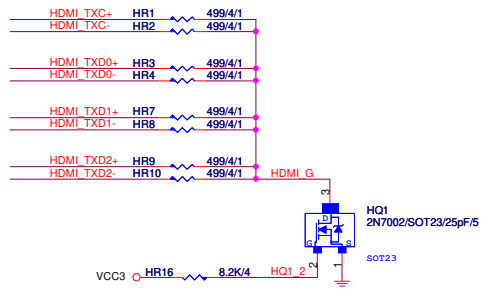








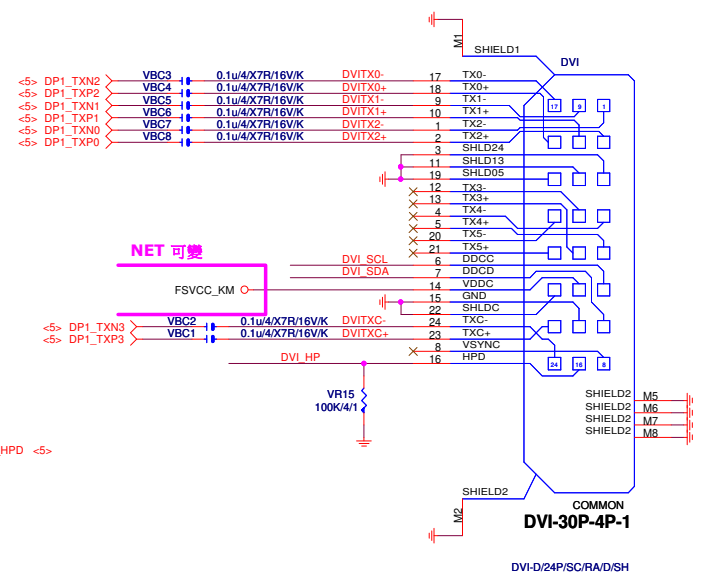
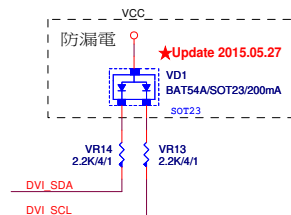
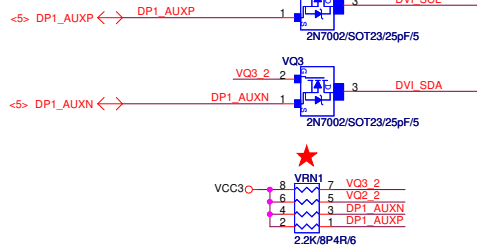
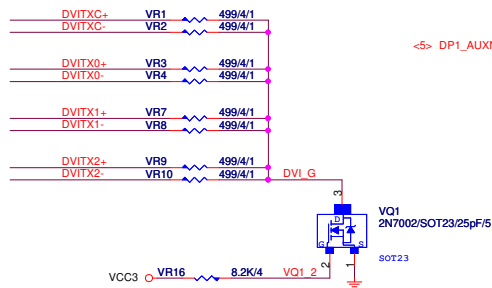




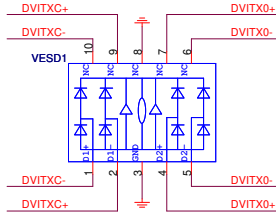
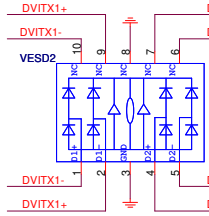
Rev: 0.73

DVI CONN

DVI: 20/4/6/4/20  
Impedance=85 +- 17.5%

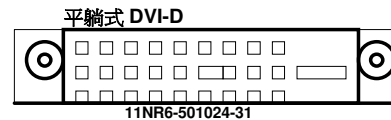


Close to connector

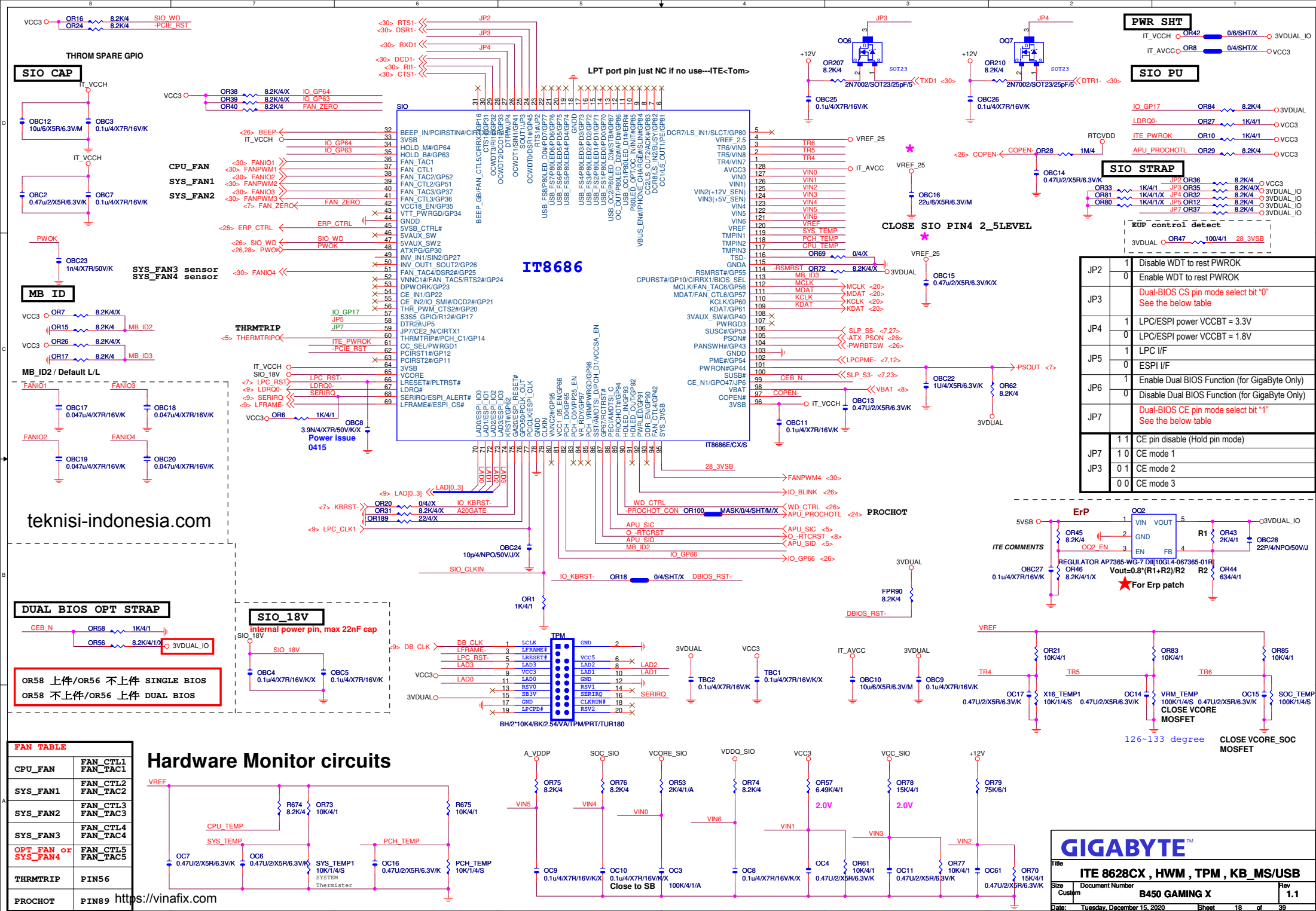


NET 可變

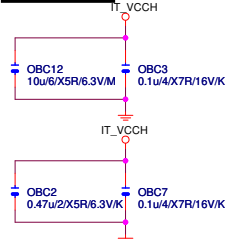
Close to connector



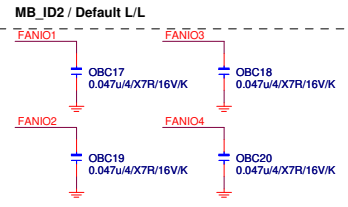
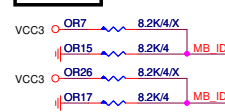
GIGABYTE™			
HDMI 2.0			
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**SIO CAP**

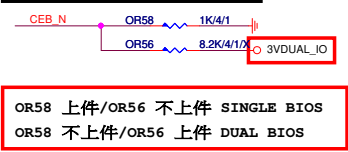


**MB ID**



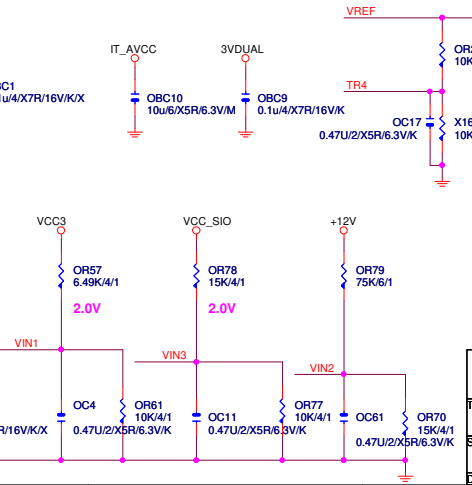
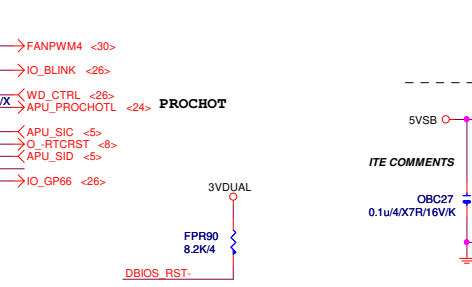
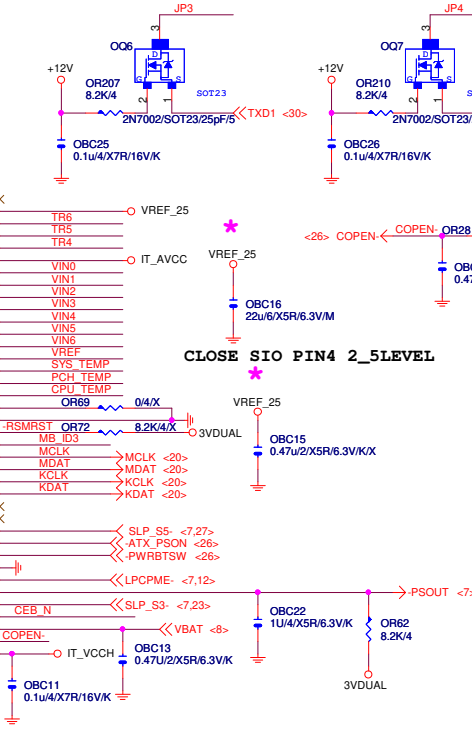
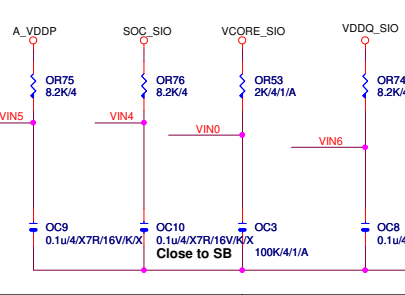
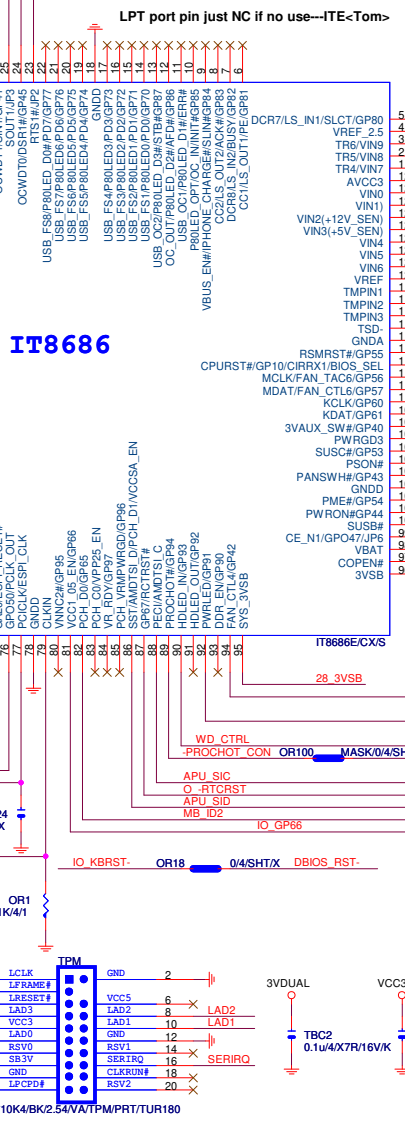
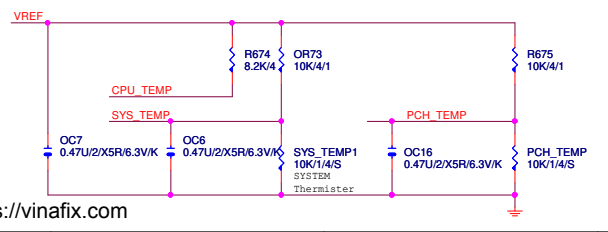
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**DUAL BIOS OPT STRAP**



FAN TABLE	
CPU_FAN	FAN_CTL1 FAN_TAC1
SYS_FAN1	FAN_CTL2 FAN_TAC2
SYS_FAN2	FAN_CTL3 FAN_TAC3
SYS_FAN3	FAN_CTL4 FAN_TAC4
SYS_FAN4	FAN_CTL5 FAN_TAC5
OPT_FAN or SYS_FAN4	FAN_CTL5 FAN_TAC5
THRMTRIP	PIN56
PROCHOT	PIN89

**Hardware Monitor circuits**



PWR SHT	
IT_VCC3	OR42 0.6/5HTX 3VDUAL_IO
IT_AVCC3	OR8 0.4/5HTX VCC3

SIO PU	
IO_GP17	OR84 8.2K/4 3VDUAL
LDRQ0	OR27 1K/4/1 VCC3
ITE_PWROK	OR10 1K/4/1 VCC3
APU_PROCHOTL	OR29 8.2K/4 VCC3

SIO STRAP	
OR33	1K/4/1 JP2 OR36 8.2K/4 VCC3
OR81	1K/4/1X JP4 OR32 8.2K/4 3VDUAL_IO
OR80	1K/4/1X JP5 OR12 8.2K/4 3VDUAL_IO
OR80	1K/4/1X JP7 OR37 8.2K/4 3VDUAL_IO

EUP control detect	
3VDUAL	OR47 100/4/1 28 3VSB

JP2	
1	Disable WDT to rest PWROK
0	Enable WDT to rest PWROK

JP3	
1	Dual-BIOS CS pin mode select bit "0"
0	See the below table

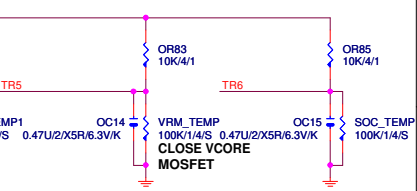
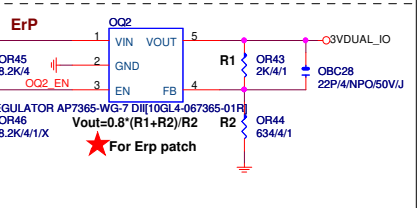
JP4	
1	LPC/ESPI power VCCBT = 3.3V
0	LPC/ESPI power VCCBT = 1.8V

JP5	
1	LPC I/F
0	ESPI I/F

JP6	
1	Enable Dual BIOS Function (for GigaByte Only)
0	Disable Dual BIOS Function (for GigaByte Only)

JP7	
1	Dual-BIOS CE pin mode select bit "1"
0	See the below table

JP7	
1 1	CE pin disable (Hold pin mode)
1 0	CE mode 1
0 1	CE mode 2
0 0	CE mode 3



**GIGABYTE**

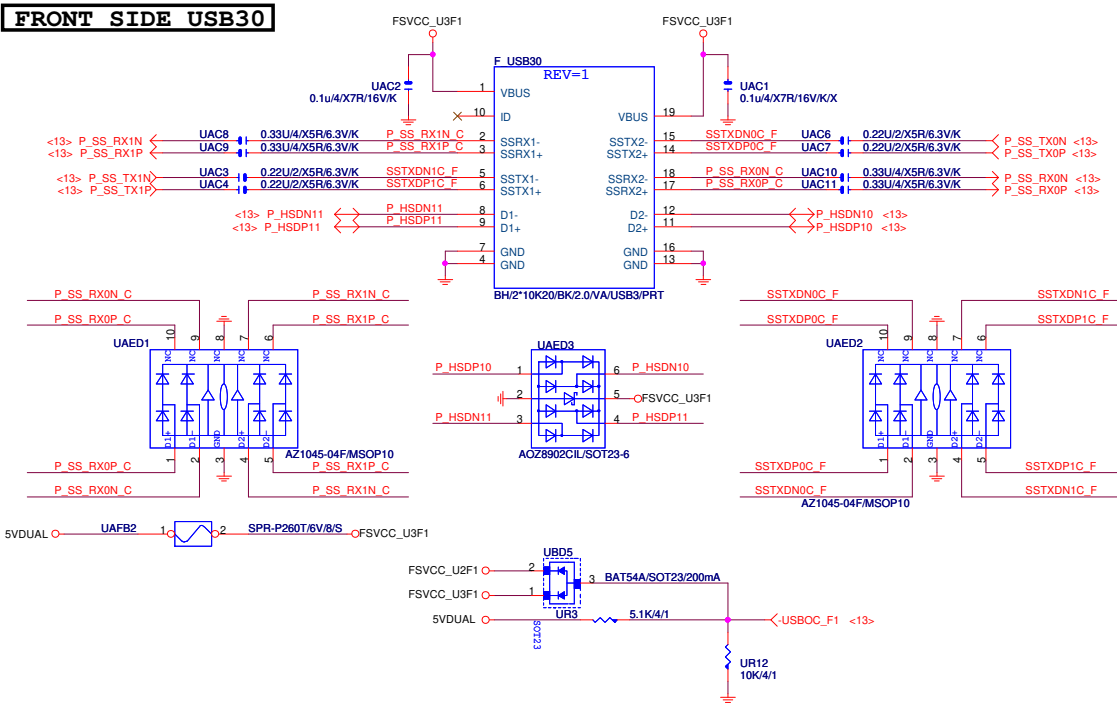
**ITE 8628CX , HWM , TPM , KB\_MS/USB**

Size: B450 GAMING X

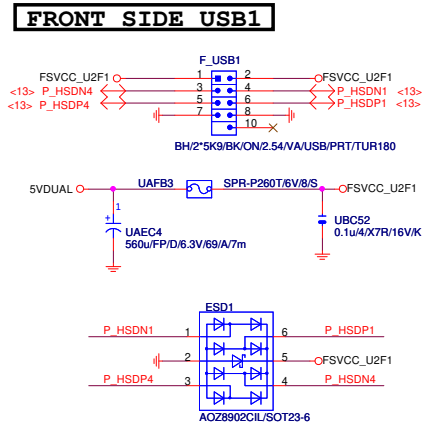
Date: Tuesday, December 15, 2020 Sheet 18 of 39

Title	ITE 8628CX , HWM , TPM , KB_MS/USB	Rev	1.1
Size	Document Number		
Custom			

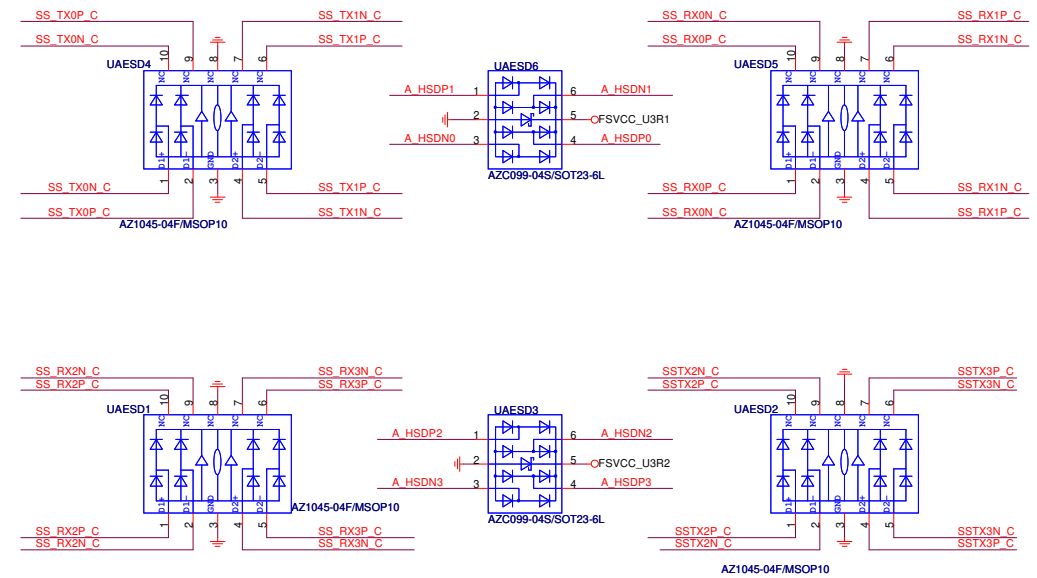
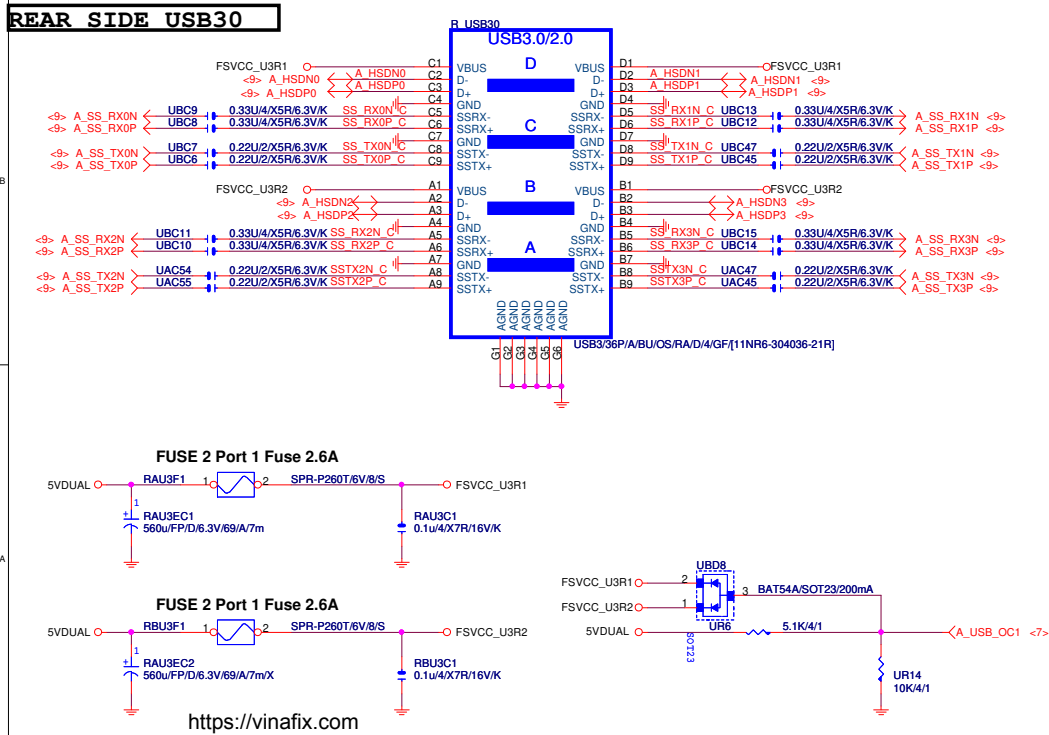
**FRONT SIDE USB30**



**FRONT SIDE USB1**



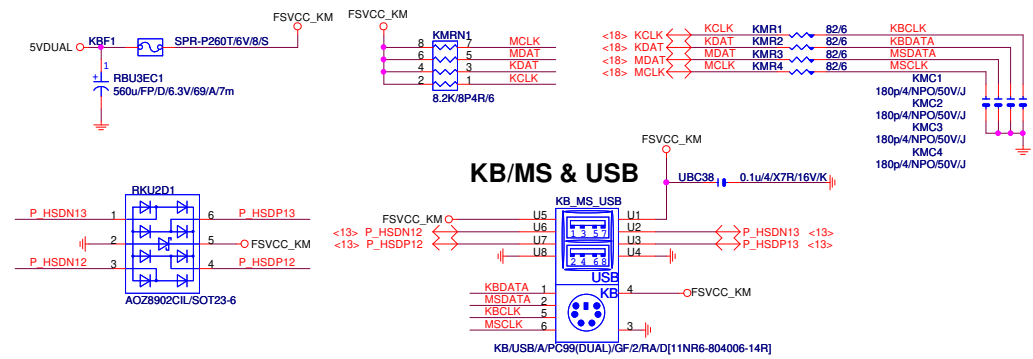
REAR SIDE USB30



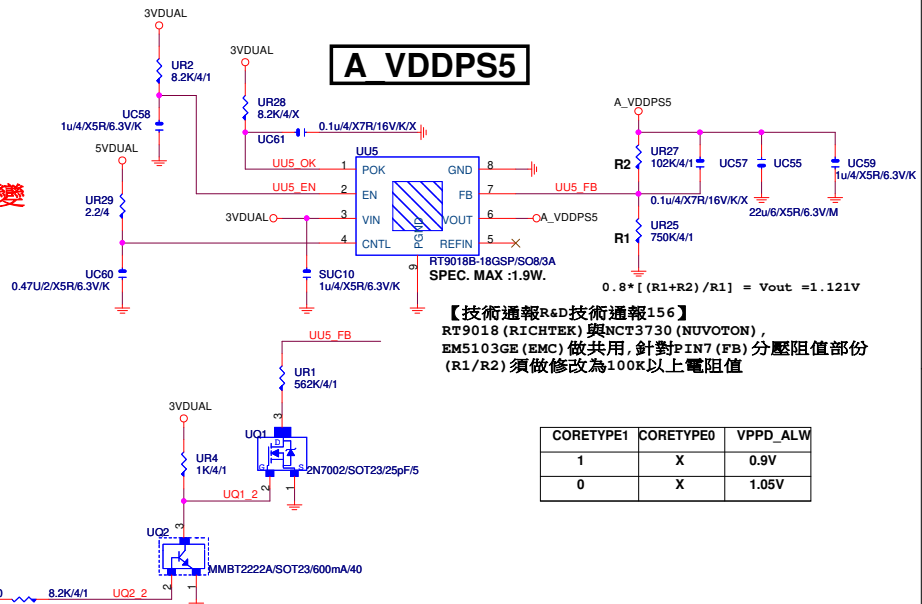
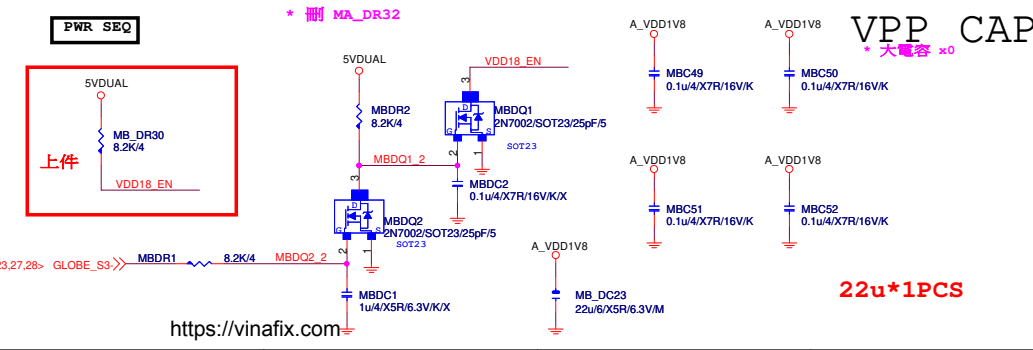
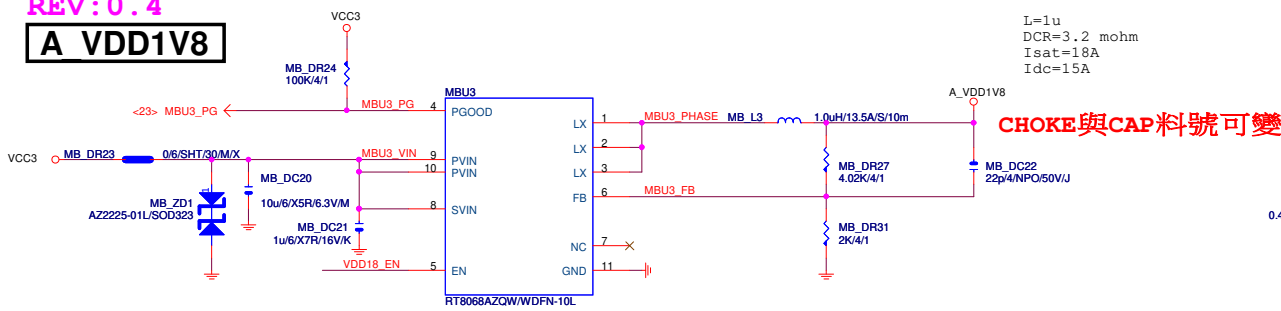
**GIGABYTE™**

Title	F_USB, R_USB CONN
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Size	Document Number	Rev
Custom	<b>B450 GAMING X</b>	<b>1.1</b>
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REV: 0.4  
**A VDD1V8**



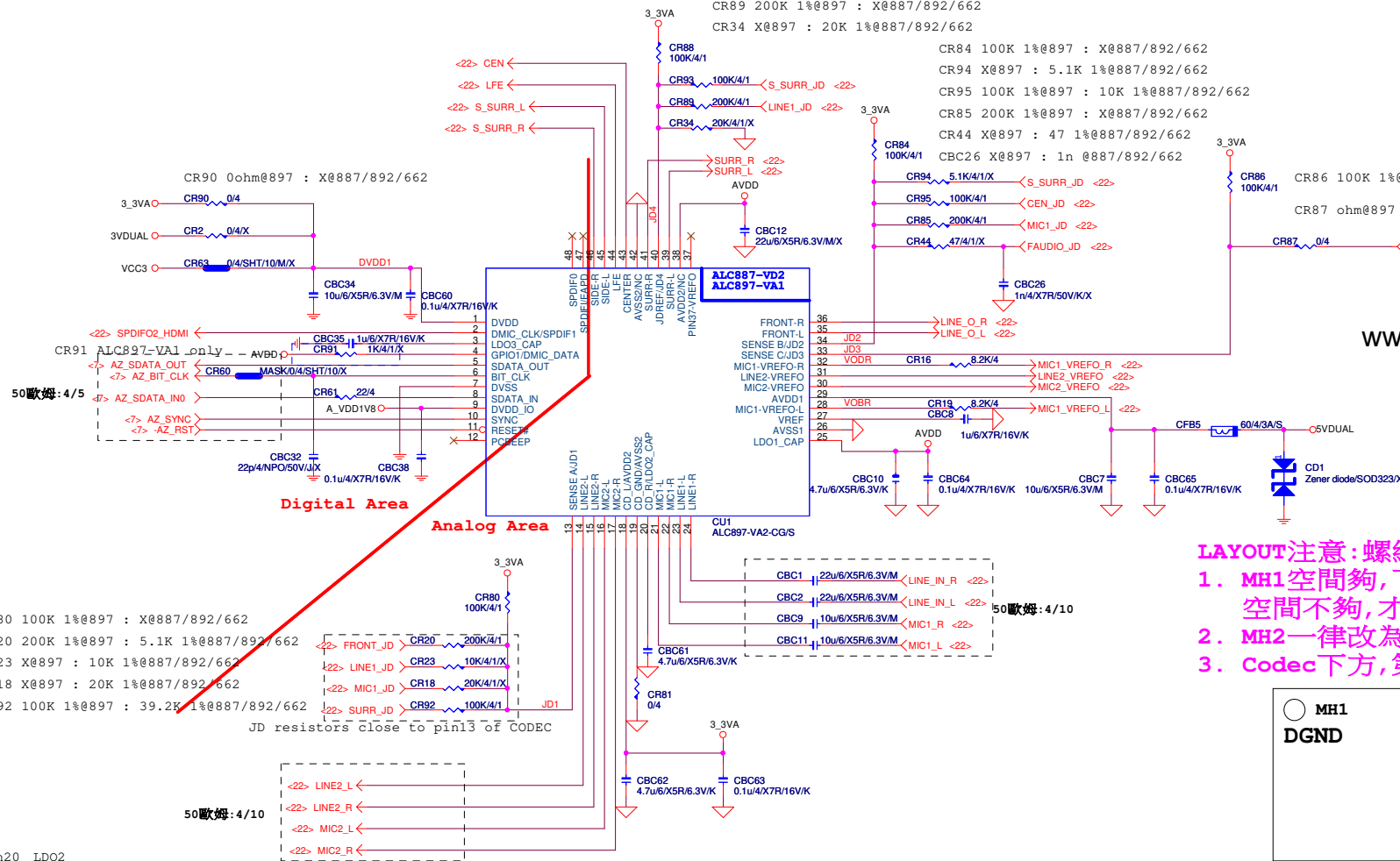
【技術通報R&D技術通報156】  
RT9018 (RICHTEK) 與NCT3730 (NUVOTON),  
EM5103GE (EMC) 做共用, 針對PIN7 (FB) 分壓阻值部份  
(R1/R2) 須做修改為100K以上電阻值

CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

CR88 100K 1%897 : X@887/892/662  
CR93 100K 1%897 : X@887/892/662  
CR89 200K 1%897 : X@887/892/662  
CR34 X@897 : 20K 1%887/892/662

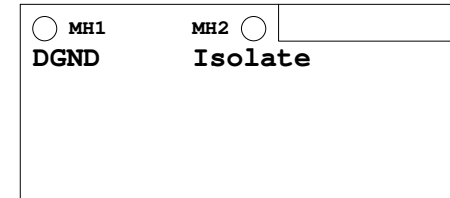
CR84 100K 1%897 : X@887/892/662  
CR94 X@897 : 5.1K 1%887/892/662  
CR95 100K 1%897 : 10K 1%887/892/662  
CR85 200K 1%897 : X@887/892/662  
CR44 X@897 : 47 1%887/892/662  
CBC26 X@897 : 1n @887/892/662

CR86 100K 1%897 : X@887/892/662  
CR87 ohm@897 : X@887/892/662



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**LAYOUT注意:螺絲孔下GND方式**  
1. MH1空間夠,下DGND  
空間不夠,才改為Isolate  
2. MH2一律改為Isolate  
3. Codec下方,第二層必須參考GND



**LAYOUT注意:要加GND切割線**

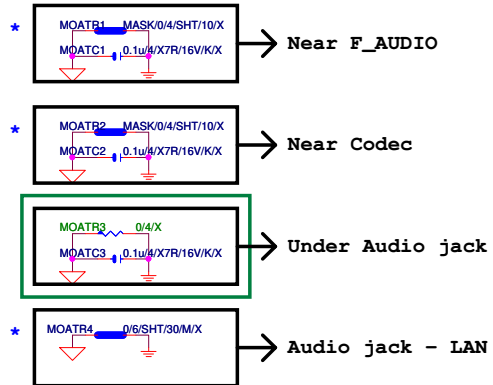
音效區域印刷



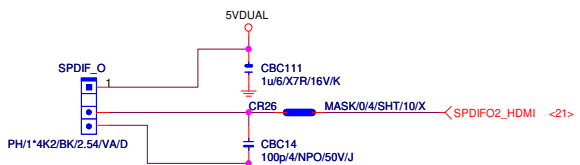
**BOM OPTION :** 1. Chemicon音效電容  
2. 金屬外罩 Reserve (LAYOUT上件與否,依照各Model spec)  
3. LED Reserve (上件與否和LED顏色,依照各Model spec)

Pin	Pin20 LDO2	897	887/892/662
Pin03	LDO3	1uF	10uF
Pin09	DVDD-IO	0.1uF	1uF
Pin18	AVDD2	4.7uF/0.1uF	NC
CR81	AVDD2	0ohm	NC
Pin20	LDO2	4.7uF	NC
Pin25	LDO1	4.7uF	22uF
Pin27	VREF	1uF	10uF
Pin38	AVDD2	NC	22uF

GIGABYTE™			
Title ALC1150 CODEC			
Size	Document Number	Rev	
Customer	B450 GAMING X	1.1	
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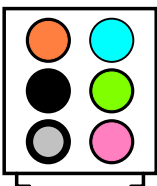


\*量産前, MOATR1/MOATR2/MOATR4 ....0ohm改short pad



For HDMI SPDIF (依SPEC保留或移除)

## AZALIA JACK



## AZALIA JACK

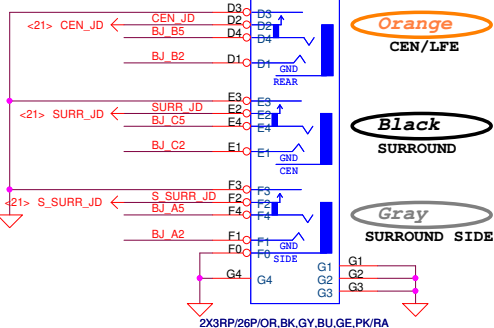
BLUE  
LINE-IN

GREEN  
LINE-OUT

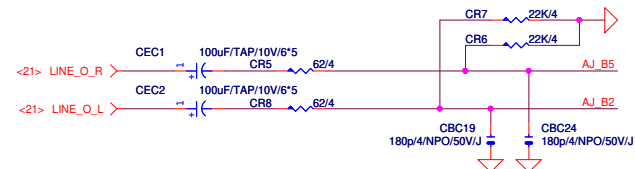
PINK  
MIC-IN

2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

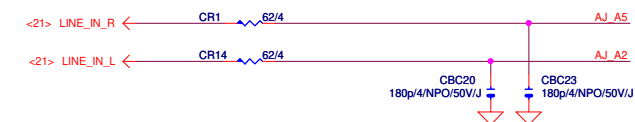
<https://vinafix.com>



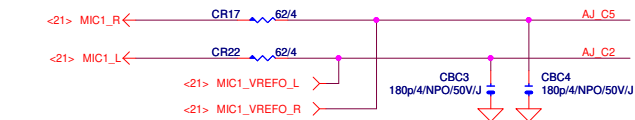
## LINE-OUT



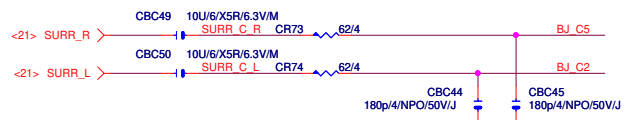
## LINE-IN



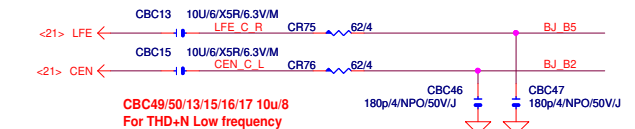
## MIC-IN



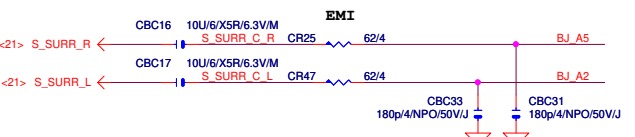
## SURROUND



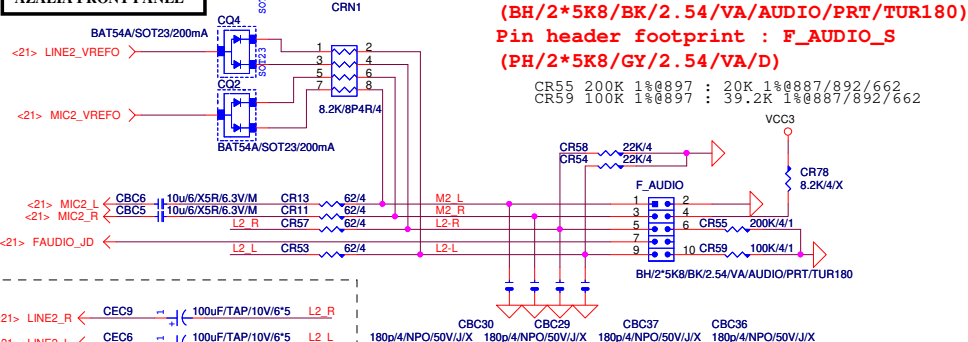
## CEN/LFE



## SURR BACK



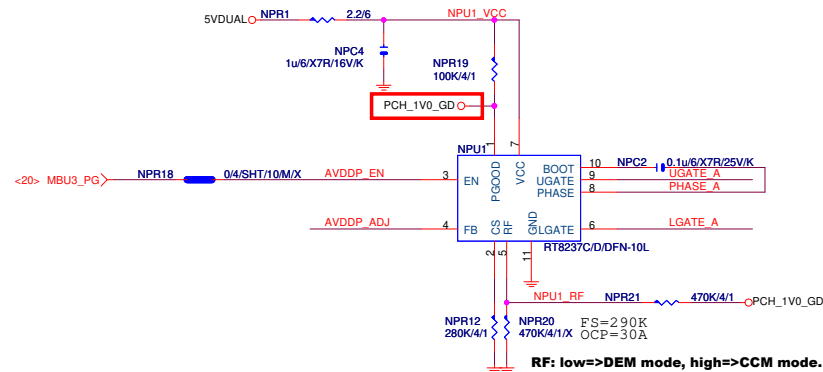
## AZALIA FRONT PANEL



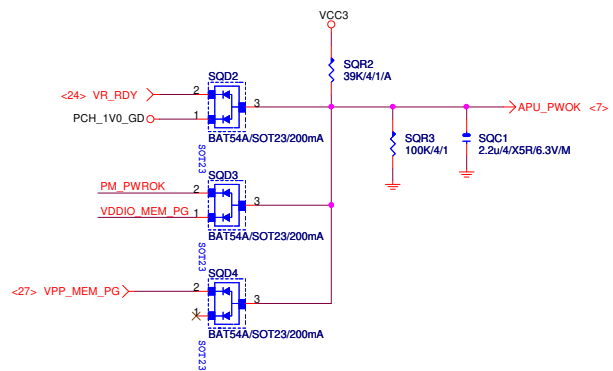
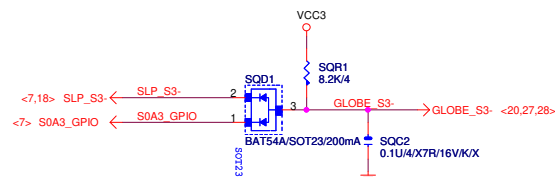
Box header footprint : F\_AUDIO  
(BH/2\*5K8/BK/2.54/VA/AUDIO/PRT/TUR180)  
Pin header footprint : F\_AUDIO\_S  
(PH/2\*5K8/GY/2.54/VA/D)

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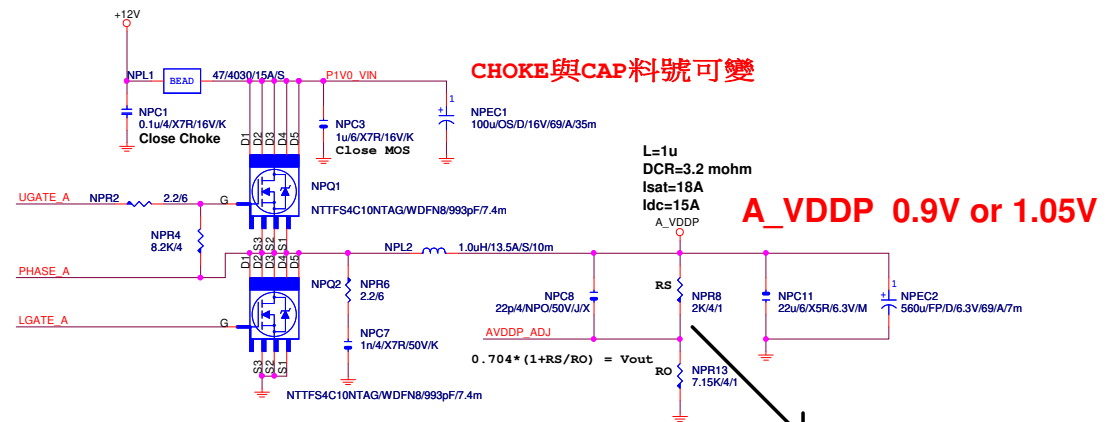
Title		
AUDIO JACK		
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**RF: low=>DEM mode, high=>CCM mode.**



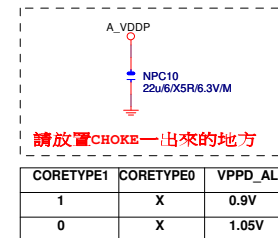
<https://vinafix.com>



**CHOKES與CAP料號可變**

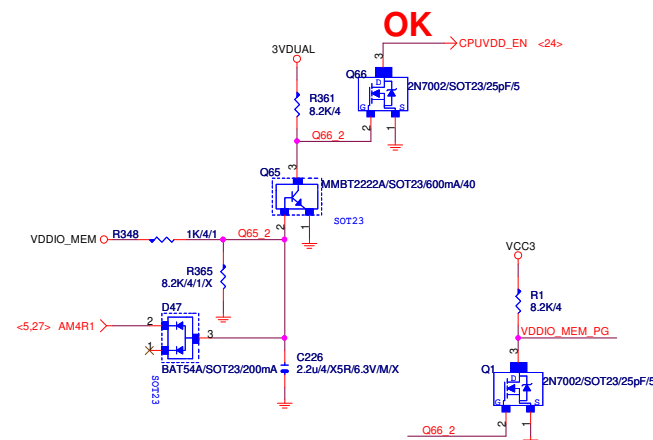
**A\_VDDP 0.9V or 1.05V**

Remote sense請從最重的負載端點拉回



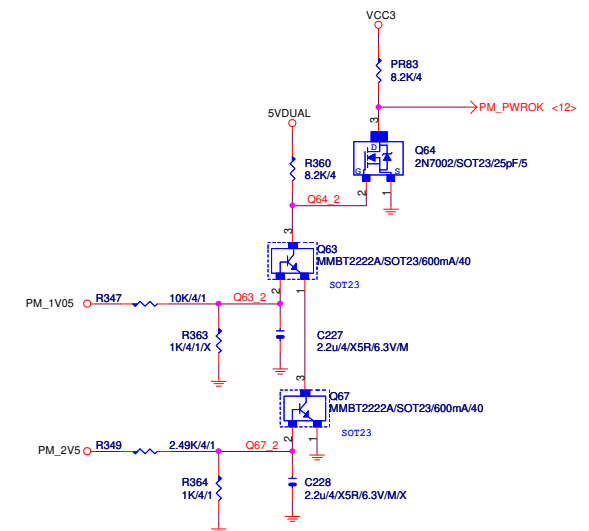
請放置CHOKE一出來的地方

CORETYPE1	CORETYPE0	VPPD_AL
1	X	0.9V
0	X	1.05V



OK

→ CPUVDD\_EN <24>

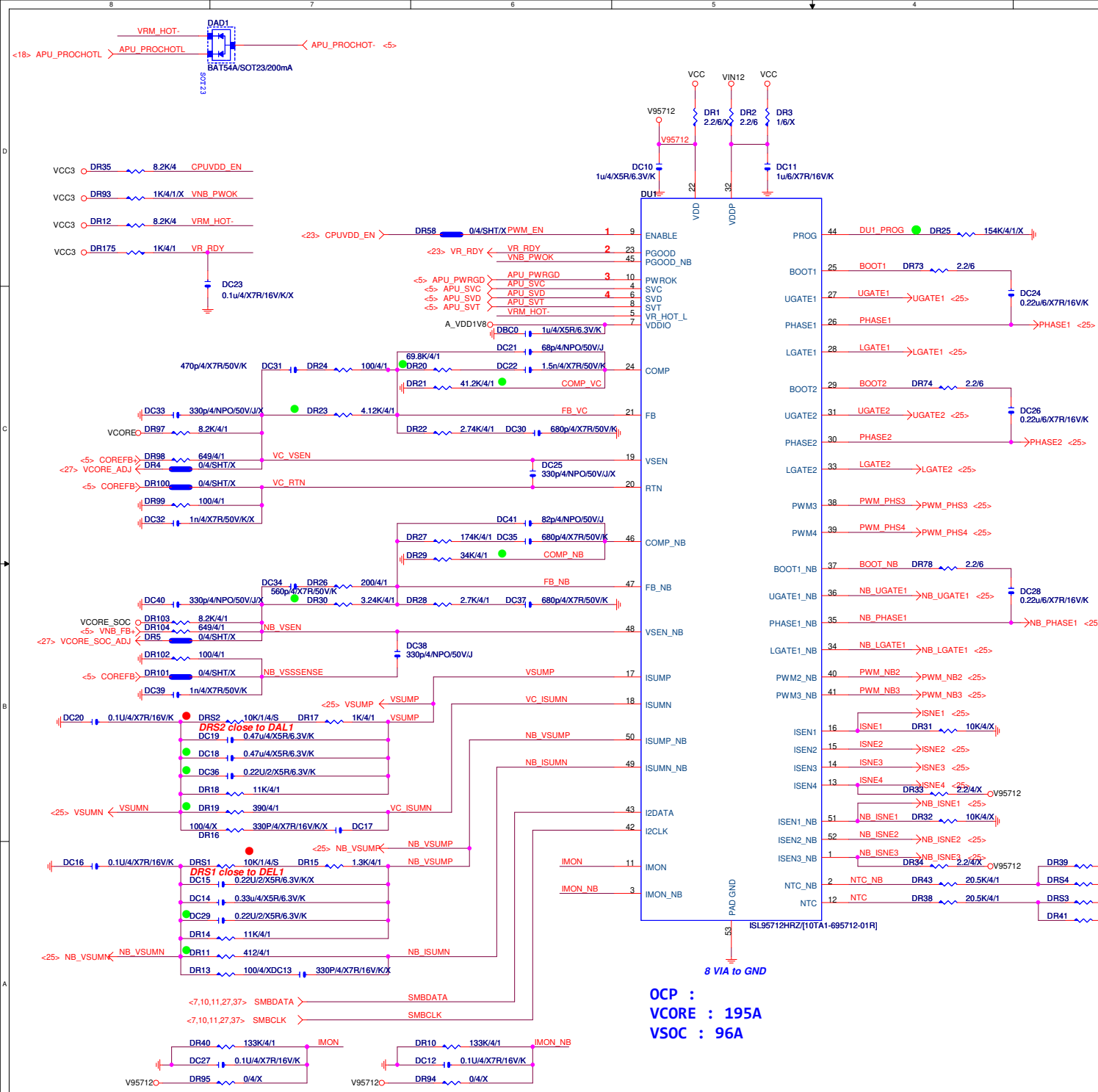


**GIGABYTE™**

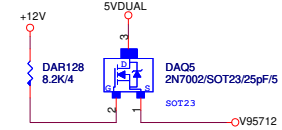
Title	<b>POWER SEQUENCE</b>
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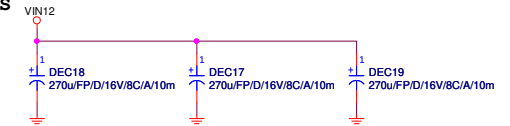




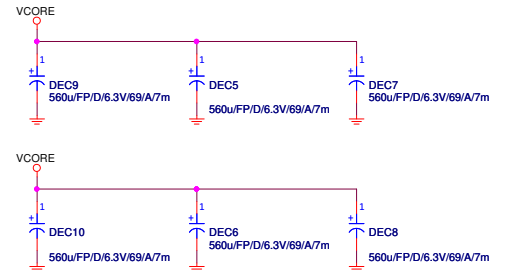
## 1. 新增DAR128.DAQ5 (12V負壓線路) 2. DR1改不上件



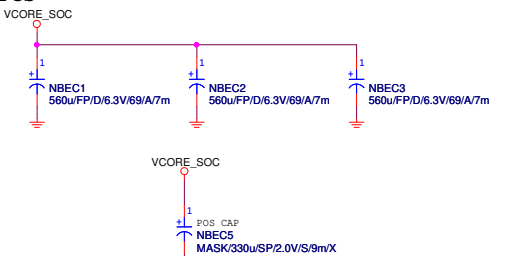
### VIN \* 3PCS



### VCORE \* 6 PCS



### VSOC \* 4 PCS



**GIGABYTE**™

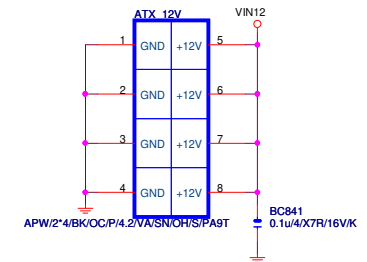
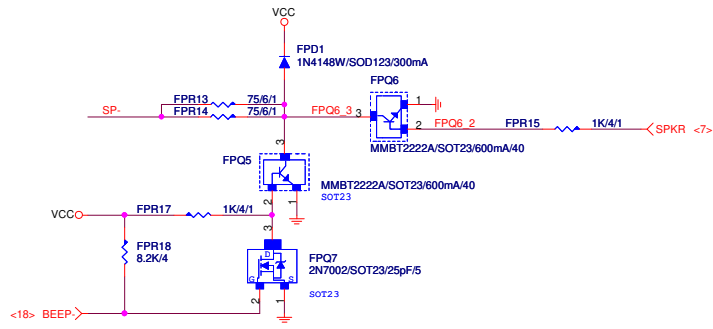
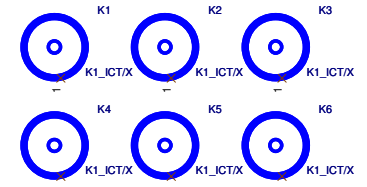
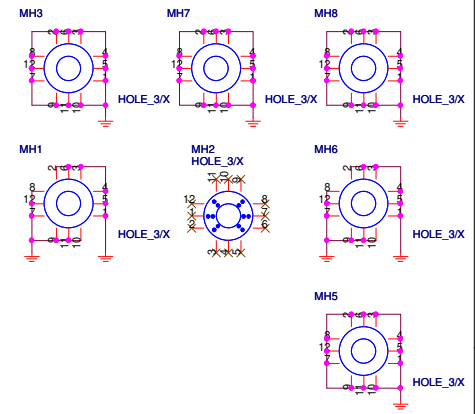
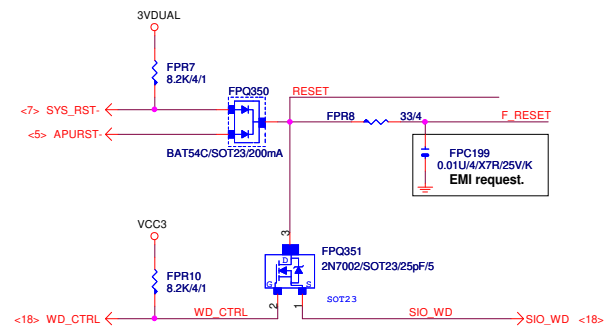
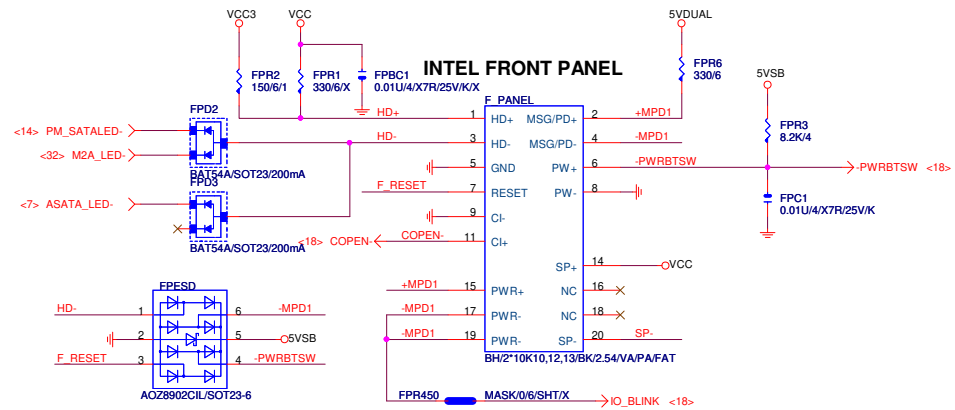
Title **VCORE (PWM ISL6277+6609A)**

Size Custom Document Number **B450 GAMING X** Rev **1.1**

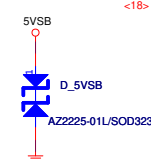
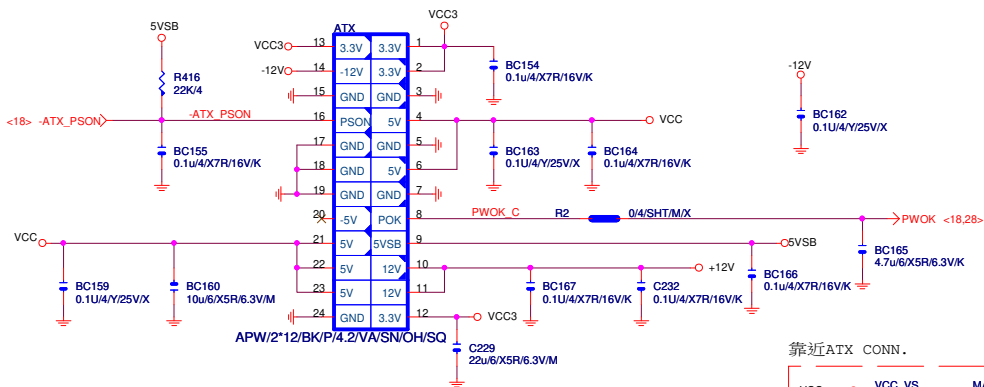
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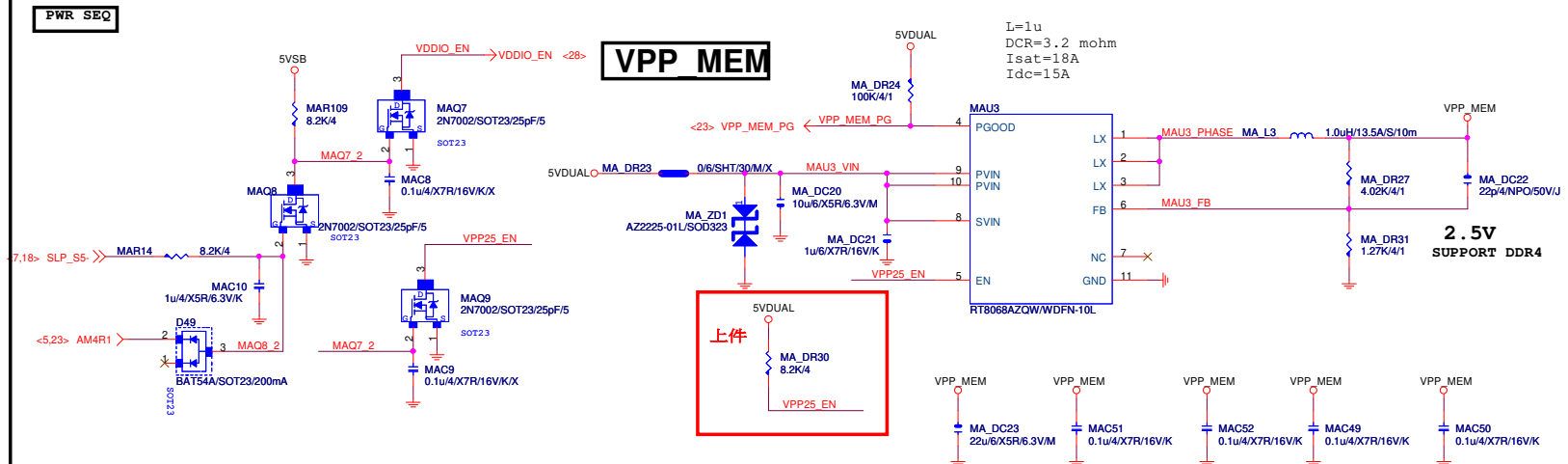
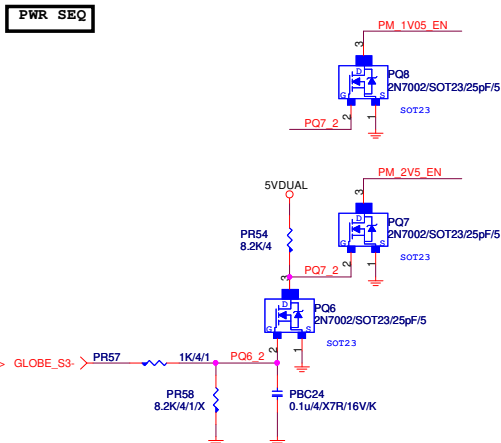
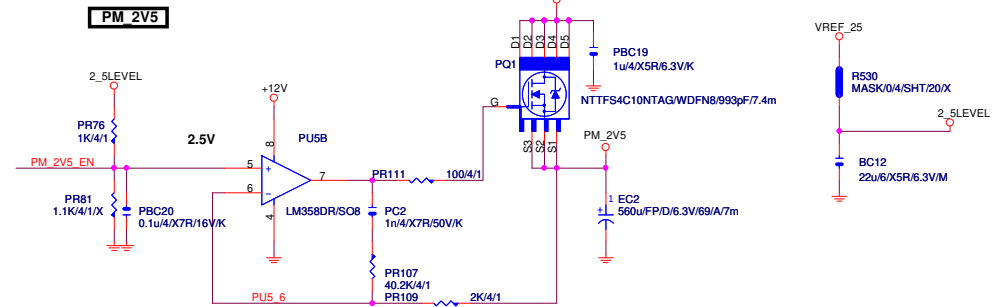
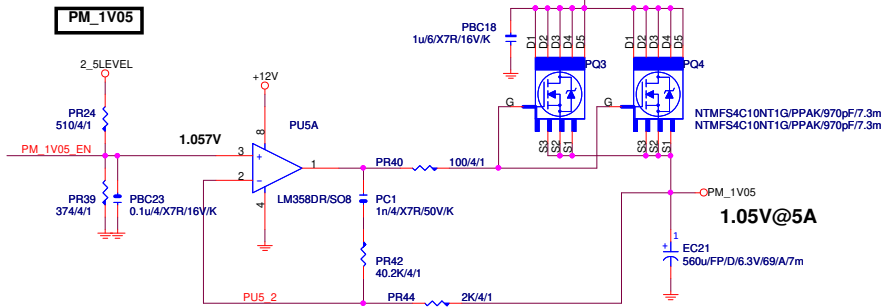


### ATX POWER CONNECTOR



## ATX, FRONT PANEL

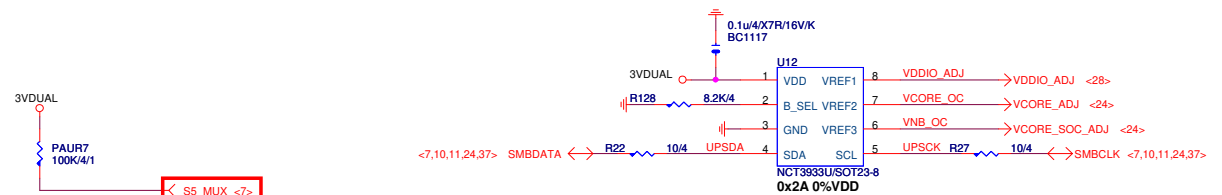
Title		Rev
B450 GAMING X		1.1
Size	Document Number	
Custom		
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## VDDCR SOC S5

S5\_MUX: S0-->High, S5-->Low  
H: VDDCR\_SOC\_S5 will track VCORE\_SOC.  
L: If VCORE\_SOC < 0.775V (OR 0.85V) , VDDCR\_SOC\_S5=0.775V.  
If VCORE\_SOC>=0.775V (OR 0.85V) , VDDCR\_SOC\_S5 will trace VCORE\_SOC.

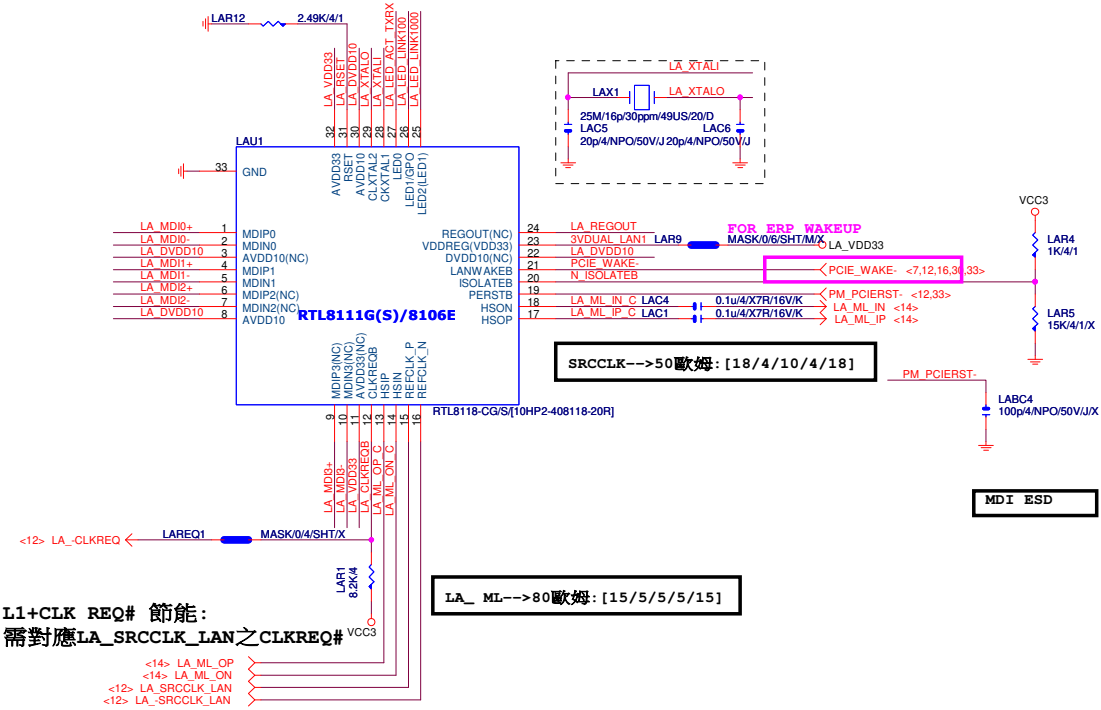
AM4 S5: 0.775V, 200mA,  
S0:VAR, 900mA.



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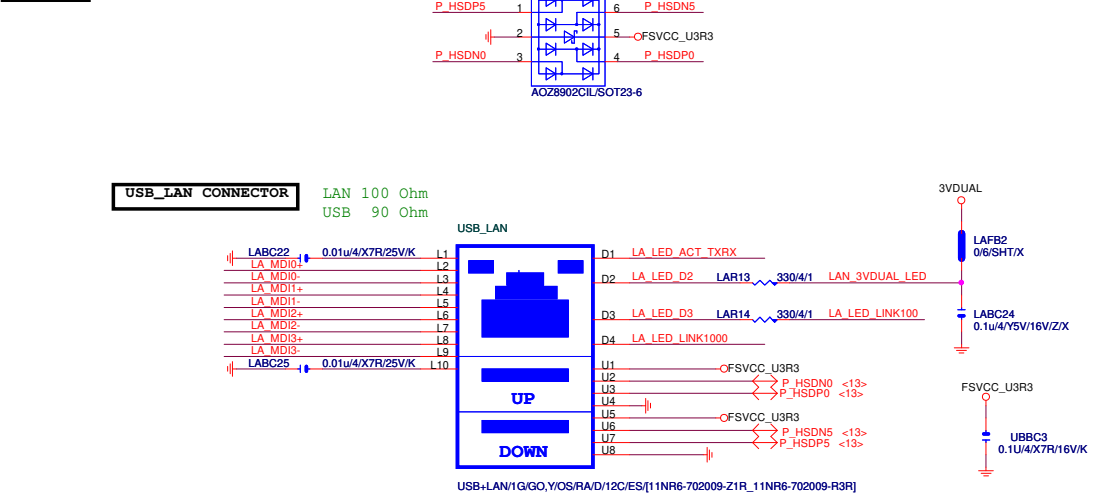
Title			
PM POWER			
Size	Document Number	Rev	
Custom	B450 GAMING X	1.1	
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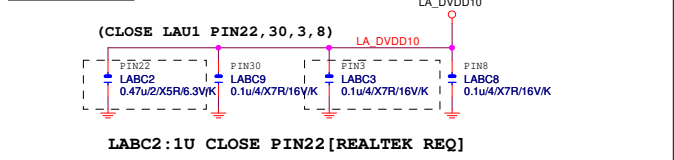
www.teknisi-indonesia.com

USB\_LAN



https://vinafix.com

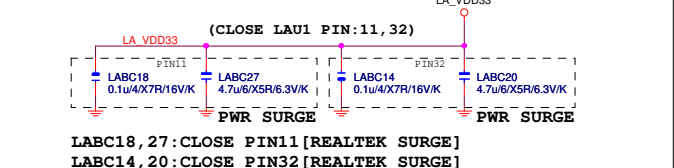
LAN POWER



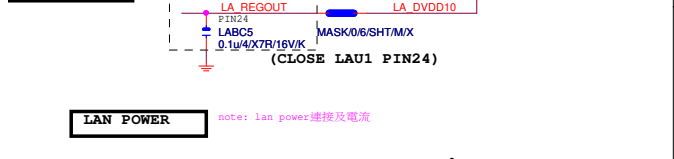
LAN POWER



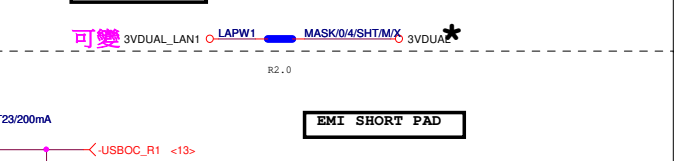
LAN POWER

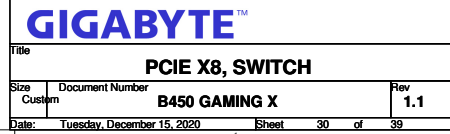
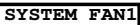


LAN POWER

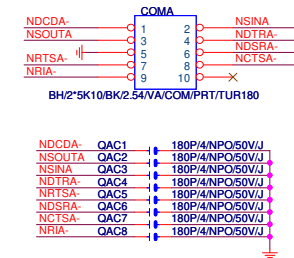


LAN POWER





## COMA

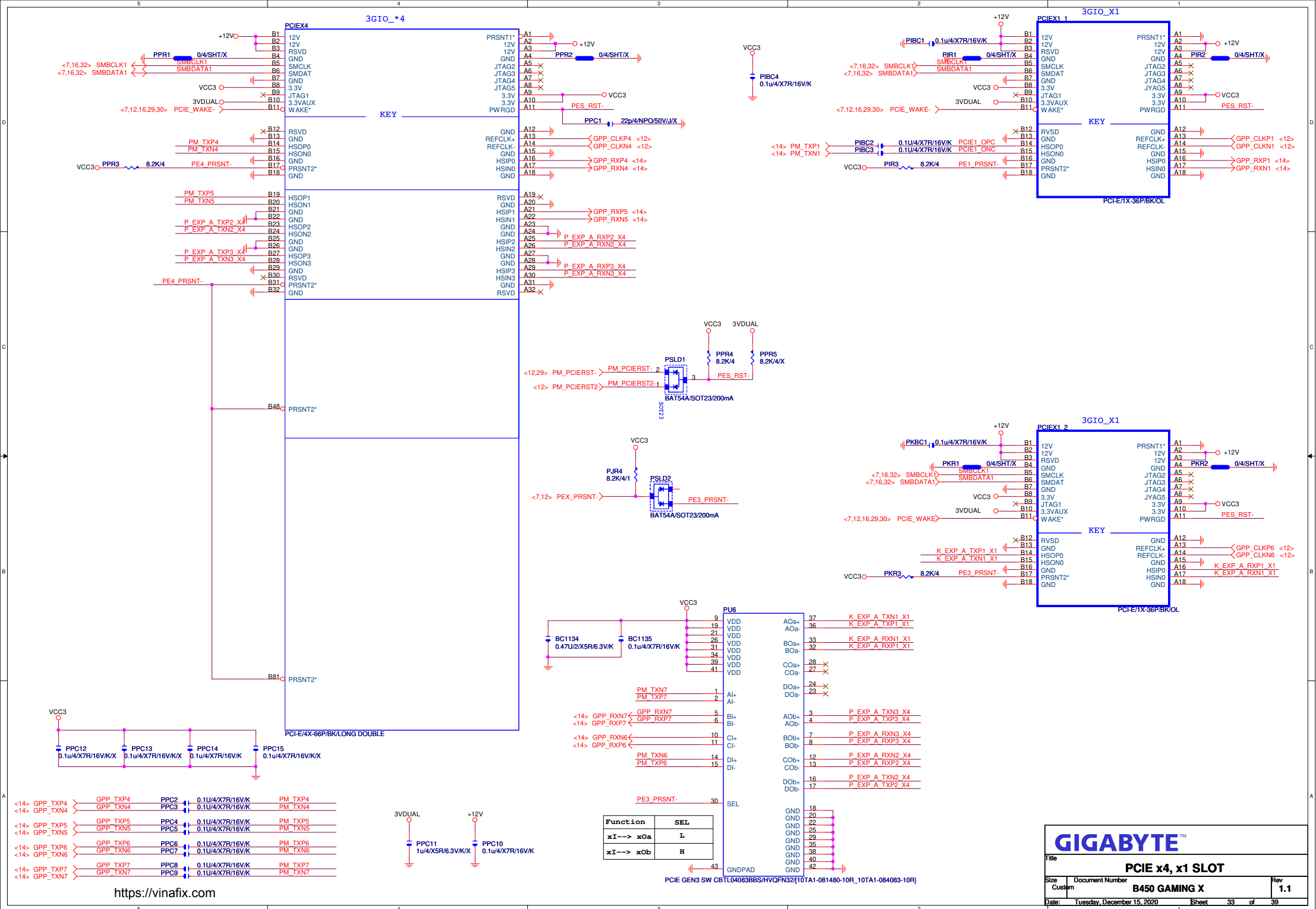


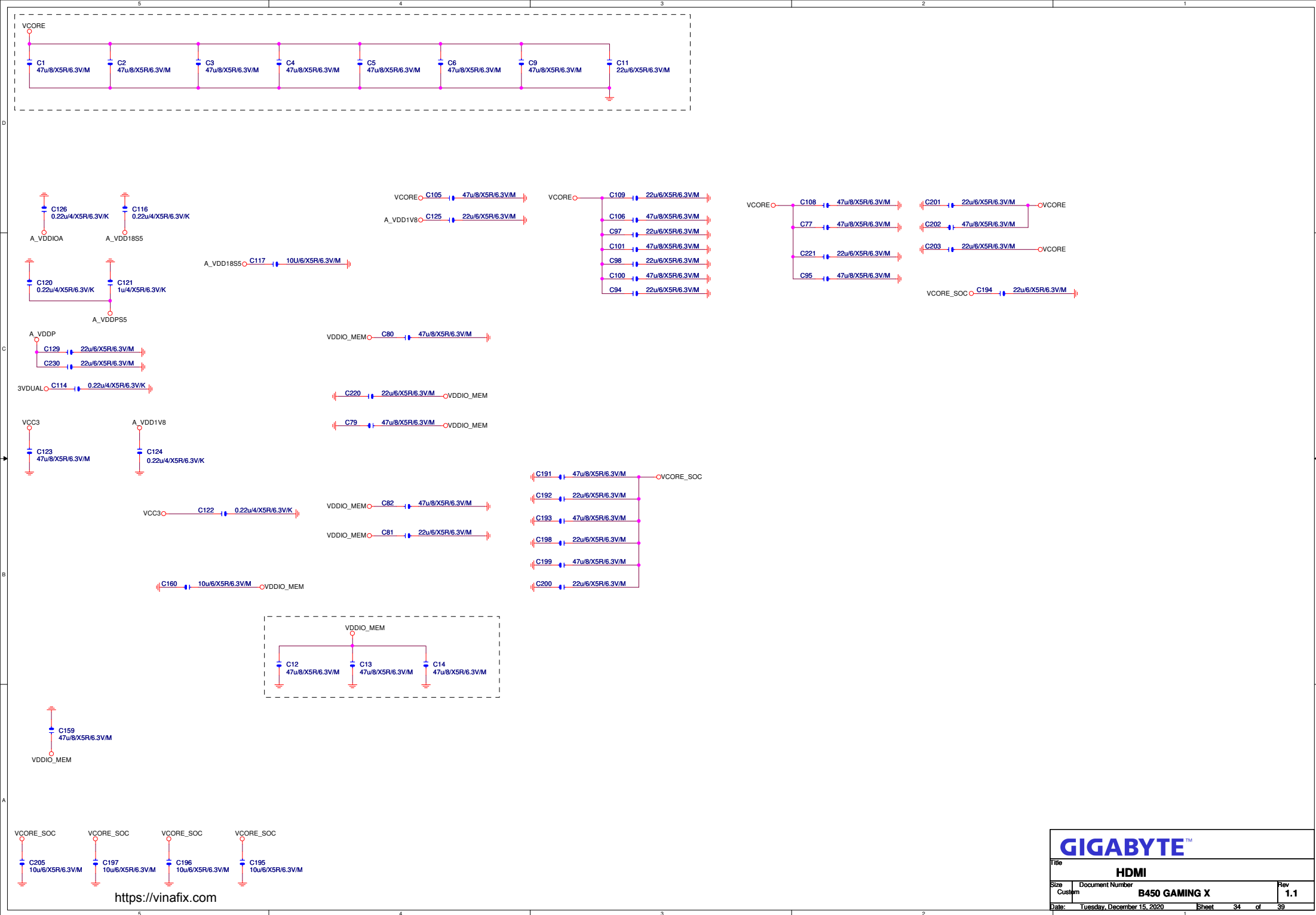
	5	4	3	2	1
D					
C					
B					
A					

<b>GIGABYTE™</b>			
Title <b>DP to VGA</b>			
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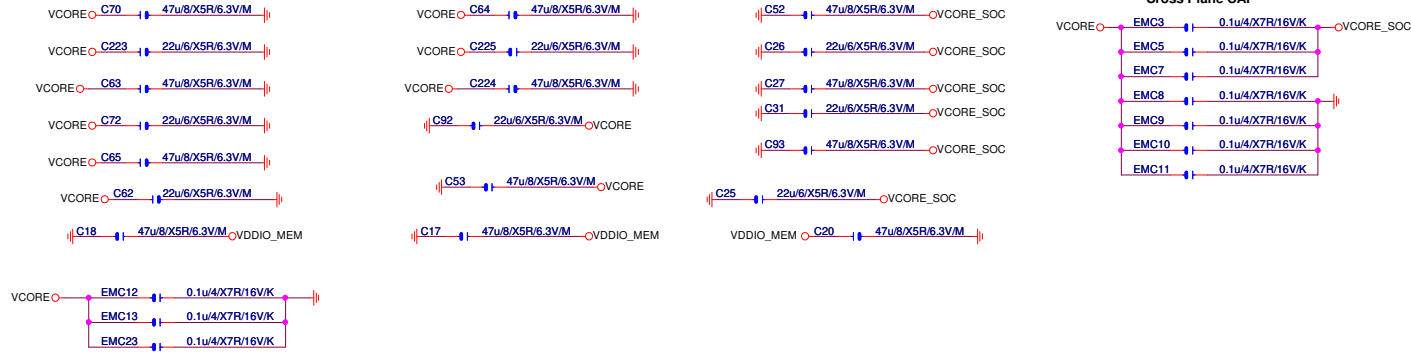








CPU TOP CAVITY





<b>GIGABYTE</b> ™			
Title			
<b>EC1</b>			
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